OMAP35x Torpedo SOM Hardware Specification

Hardware Documentation

Logic PD // Products
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Revision History

REV	EDITOR	REVISION DESCRIPTION	SCHEMATIC PN & REV	APPROVAL	DATE
1	NJK	-Preliminary Release	1012512 Rev B	NJK	04/22/09
2	JCA	-Added drawings to end of document	1012512 Rev B	JCA	05/27/09
A	JCA, NJK	-Throughout: Added references to AN 416 and WP 419 documents where appropriated; added direct links to documents in Section 1.3;removed “PRELIMINARY DOCUMENT” markings; -Table 3.1: Added DC USB1_VBUS Input Voltage to table; -Table 3.2: Added DC Main Battery Currents; Added DC USB1_VBUS Input Voltage; Updated DC 5 V Voltage Min & Typical numbers; Added notes 5-9 to explain how the power numbers were obtained; -Table 4.1: Changed Torpedo SOM Net Name for SDRC_CLK to N/A; -Section 5.6.1: Added Section for USB1_VBUS; Updated 5V Section to reference AN416 and battery charging; -Section 7: Added Important Note regarding reference voltages; -Section 7.2: J2.52, J2.54, J2.56, J2.58 updated reference voltage to be 1.8V and added table notes 3, 4, & 5 to address special use scenarios for these signals; -Section 2.3.2: Changed heading and referenced WP419; -Appendix A: Attached updated mechanical drawings	1013989 Rev A	NJK	02/18/10
B	JCA	-Section 4.5.5.1: added reserved I2C addresses; -Section 7.2: J2.85, J2.87 added voltage reference to VAUX4 and added notes to the description;	1013989 Rev A	RH	04/21/10
C	SMC, KH	-Table 3.2: Updated typical active current numbers for 4.0V; Added WinCE suspend current numbers; Added note 11 about minimum and maximum values; -Section 4.2.1: Updated available densities; -Sections 4.7 & 4.8 Added Design Note ; -Section 7.1 Added Notes for PoP related signals; -Sections7.3 7.1, 7.2, & 7.3: Added BGA Ball # and Processor Signal columns; -Section 7.2: Pin J2.32, removed requirement for 10K pull-up	1013989 Rev B	NJK	03/31/11
D	SO	-Throughout: Updated template; updated links for new support site; reorganized a few sections; -Added Table 2.1 regarding mechanical specifications; -Added Section 2.3.3 regarding pick and place recommendations; -Section 5.4: Revised reference to ETM reference design; -Section 4.6: Added note that proper USB adapter cable is necessary for USB 2.0 OTG to function as host; added link to Digi-Key adapter cable that supports host function; -Appendix A: Updated mechanical drawing	1013989 Rev B	RAH, NJK	11/14/13
E	SO	-Added Section 2.3.4 regarding recommended insertion procedures to ensure correct insertion of SOM	1013989 Rev B	RAH	12/18/13

Please check the Logic PD support site[1] for the latest revision of this specification and additional documentation.

[1] http://support.logicpd.com/Home.aspx

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1 Introduction

1.1 Product Overview

The Torpedo System on Module (SOM) is an ultra-compact form factor based on Texas Instruments' OMAP35x processor family.

The Torpedo SOM provides a module solution for applications that require low-power and high-performance within tight space constraints. When compared to equivalent OMAP 0.65 mm BGA package and external memory solutions, the Torpedo SOM requires 45% less surface area and 12% less volume.

As an off-the-shelf solution, the Torpedo SOM reduces development risks associated with the complex design and manufacturing details of the OMAP 3 processor. It leverages Package-on-Package (PoP) technology to place the on-board memory on top of the processor. Though the PoP process requires additional PCB layers, those extra layers are confined to the dime-sized SOM; this allows customers to use PCB with fewer layers for their baseboards, thereby lowering the overall PCB and manufacturing costs. The Torpedo SOM form factor also allows developers to reuse existing baseboard designs when upgrading to new OMAP processors, which extends roadmap possibilities for their end-product.

The ultra-compact Torpedo SOM is ideal for applications in the medical, point-of-sale, industrial, security, and consumer markets where space is at a premium. From point of care medical devices to bar code readers, handheld radios to mobile Internet devices, netbooks to CCTV cameras, the Torpedo SOM allows for powerful versatility, compact designs, and long-life products.

By starting with the corresponding Zoom OMAP35x Torpedo Development Kit, engineers can write application software on the same hardware that will be used in the final product. The standard Torpedo SOM features the OMAP3530 processor, but also supports the OMAP3503 processor.

NOTE: Within this document, OMAP35x is used to denote either the OMAP3530 or OMAP3503 processor. Also, it can be assumed that OMAP35x and OMAP35xx hold the same meaning.

1.2 Abbreviations, Acronyms, and Definitions

ADC	Analog to Digital Converter
BSP	Board Support Package
BTB	Board-to-Board
DDR	Double Data Rate (RAM)
DMA	Direct Memory Access
ESD	Electrostatic Discharge
FIFO	First In First Out
GPIO	General Purpose Input Output
GPMC	General Purpose Memory Controller
GPO	General Purpose Output
I2C	Inter-Integrated Circuit
I2S	Inter-Integrated Circuit Sound
IC	Integrated Circuit
I/O	Input/Output

IRQ	Interrupt Request
LCD	Liquid Crystal Display
LDO	Low Dropout (Regulator)
McBSP	Multi-channel Buffered Serial Port
OTG	On-the-Go (USB)
PCB	Printed Circuit Board
PCMCIA	Personal Computer Memory Card International Association (PC Cards)
PHY	Physical Layer
PLL	Phase Lock Loop
PoP	Package on Package
PWM	Pulse Width Modulation
RTC	Real Time Clock
SDIO	Secure Digital Input Output
SDRAM	Synchronous Dynamic Random Access Memory
SOM	System on Module
SSP	Synchronous Serial Port
SPI	Standard Programming Interface
STN	Super-Twisted Nematic (LCD)
TFT	Thin Film Transistor (LCD)
TI	Texas Instruments
TSC	Touch Screen Controller
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receive Transmit

1.3 Scope of Document

This hardware specification is unique to the design and use of the OMAP35x SOM Torpedo as designed by Logic PD and does not intend to include information outside of that scope. Detailed information about the Texas Instruments (TI) OMAP35x processors or any other device component on the SOM can be found in their respective manuals and specification documents.

1.4 Additional Documentation and Resources

The following documents and documentation resources have been referenced throughout this hardware specification:

- TI's *OMAP35x Technical Reference Manual (TRM)*[2]
- TI's *OMAP3530/25 Applications Processor Datasheet*[2]
- TI's *TPS65950 OMAP Power Management and System Companion Device TRM*[3]
- TI's *TPS65950 Data Manual*[3]
- *USB 2.0 Specification*[4] available from USB.org
- Logic PD's *LogicLoader v2.4 User Manual*[5]
- Logic PD's *OMAP35x Torpedo SOM LogicLoader User Manual Addendum*[6]
- Logic PD's *AN 416 OMAP35x Torpedo SOM Power Management*[7]
- Logic PD's *WP 419 Torpedo SOM Mechanical Hold-Down Scenarios*[8]
- Logic PD's Hardware Design Files (BOM, Schematic, and Layout) for all boards included in the development kit (baseboard, SOM, LCD), as well as all standard configuration SOMs. Sign into your account on Logic PD's support site[9] to access these files.

[2] http://www.ti.com/product/omap3530
[3] http://www.ti.com/product/tps65950#technicaldocuments
[4] http://www.usb.org/developers/docs/
[5] http://support.logicpd.com/DesktopModules/Bring2mind/DMX/Download.aspx?portalid=0&EntryId=1455
[6] http://support.logicpd.com/DesktopModules/Bring2mind/DMX/Download.aspx?portalid=0&EntryId=972
[7] http://support.logicpd.com/DesktopModules/Bring2mind/DMX/Download.aspx?portalid=0&EntryId=964
[8] http://support.logicpd.com/DesktopModules/Bring2mind/DMX/Download.aspx?portalid=0&EntryId=984

2 Functional Specification

2.1 OMAP35x Processor Highlights

The OMAP35x Torpedo SOM uses TI's high-performance OMAP35x Applications Processor. This device features the Superscalar ARM® Cortex™-A8 RISC core and provides many integrated on-chip peripherals, including:

- Superscalar ARM® Cortex™-A8 RISC core
  - Vectored floating point unit
  - 16 Kbytes instruction L1 cache
  - 16 Kbytes data L1 cache
  - 256 Kbyte L2 cache
  - 64 Kbyte RAM
  - 32 Kbyte ROM
- Integrated LCD Controller
  - Up to 1024 x 768 x 24 bit color
- Three UARTs
- I2S codec interface
- One high-speed USB 2.0 On-the-Go (OTG) interface and one high-speed USB 2.0 host interface
- Many general purpose I/O (GPIO) signals
- Programmable timers
- Real time clock (RTC)
- Low power modes

See TI's *OMAP35x TRM* and *OMAP3530/25 Applications Processor Datasheet* for additional information.

IMPORTANT NOTE: Please visit TI's website[10] for errata on the OMAP35x processor.

[9] http://support.logicpd.com/Home.aspx
[10] http://www.ti.com/product/omap3530

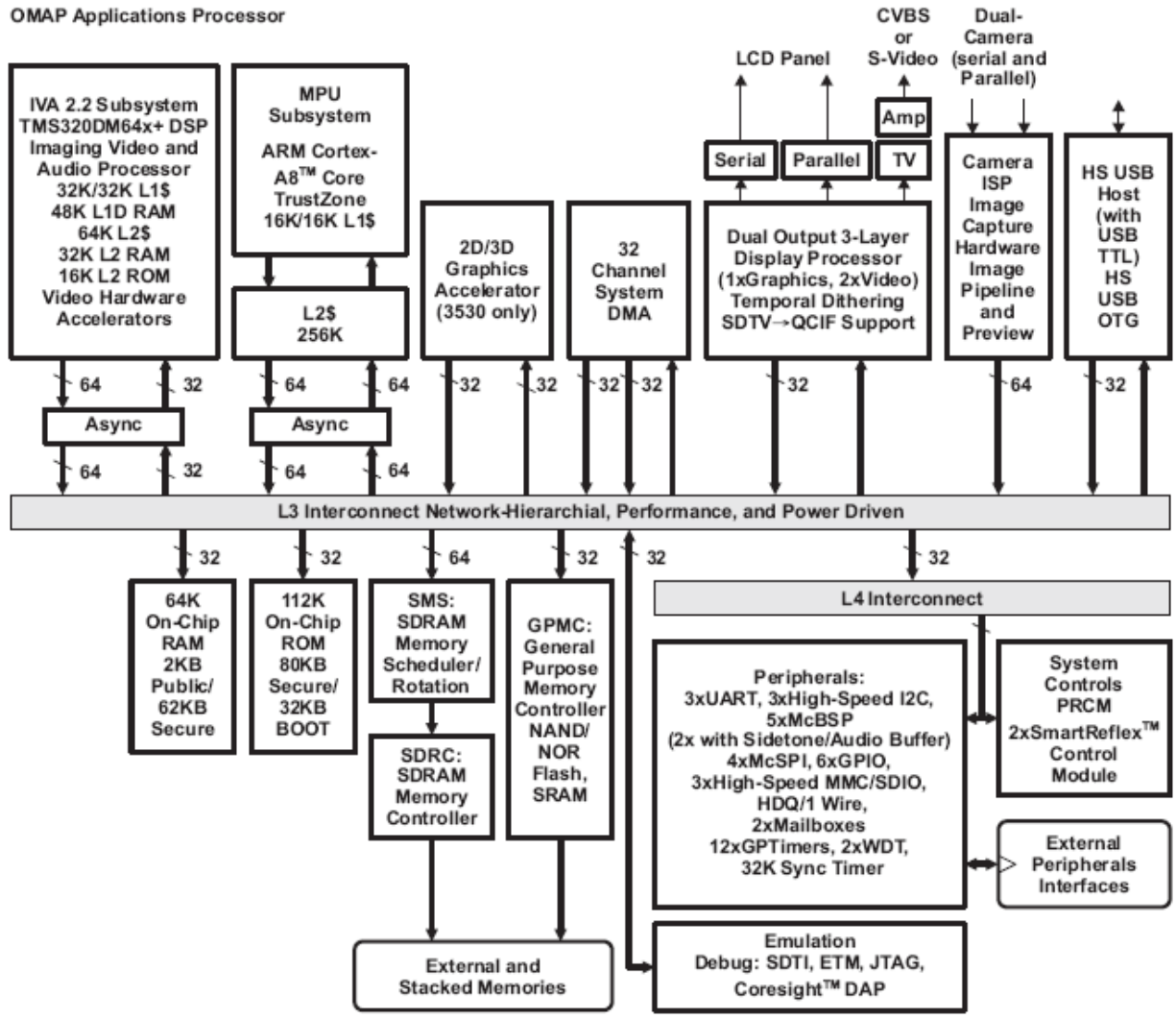


Figure 2.1: OMAP35x Processor Block Diagram

NOTE: The block diagram pictured above comes from TI's *OMAP3530/25 Applications Processor Datasheet.*

2.2 Torpedo SOM Interface

Logic PD's common Torpedo SOM interface allows for easy migration to new processors and technology. Logic PD is constantly researching and developing new technologies to improve performance, lower cost, and increase feature capabilities. By using the common Torpedo SOM footprint, it may be possible to take advantage of Logic PD's work without having to re-spin the old design.

In fact, encapsulating a significant amount of your design onto the Torpedo SOM reduces any long-term risk of obsolescence. If a component on the Torpedo SOM design becomes obsolete, Logic PD will design for an alternative part that is transparent to your product. Furthermore, Logic PD tests all SOMs prior to delivery, decreasing time-to-market and

ensuring a simpler and less costly manufacturing process. Contact Logic PD[11] for more information.

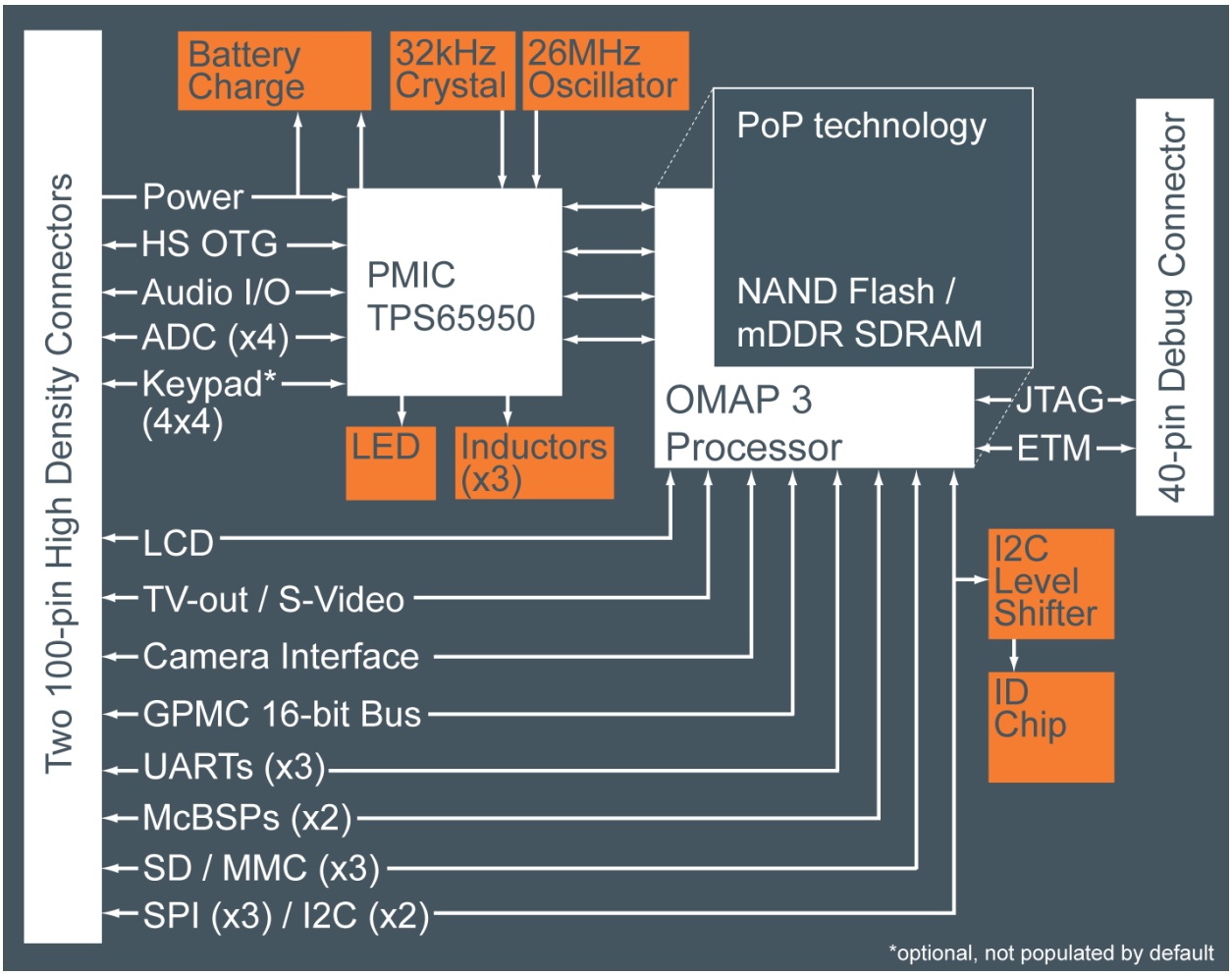


Figure 2.2: OMAP35x Torpedo SOM Block Diagram

2.3 Mechanical Specification

Table 2.1: Mechanical Characteristics of SOM

Parameter	Min	Typical	Max	Unit	Notes
Dimensions	—	15.0 x 27.0 x 3.8	—	mm	—
Weight	—	1.96	—	Grams	1
Connector Insertion/Removal	—	30	—	Cycles	—

TABLE NOTES:

1. May vary depending on SOM configuration.

[11] http://support.logicpd.com/TechnicalSupport/AskAQuestion.aspx

The OMAP35x Torpedo SOM connects to a PCB baseboard through two 100-pin board-to-board (BTB) socket connectors.

Table 2.2: Baseboard Mating Connectors

Ref Designator	Manufacturer	Torpedo Connector P/N	Mating Connector P/N
J1, J2	Hirose	DF40C-100DP-0.4V(51)	DF40C-100DS-0.4V(51)

2.3.1 OMAP35x Torpedo SOM Mechanical Drawings

Please see Appendix A for mechanical drawings of the OMAP35x Torpedo SOM and recommended baseboard footprint layout.

2.3.2 Example OMAP35x Torpedo SOM Retention Methods

Logic PD has developed several methods to secure the OMAP35x Torpedo SOM in an end product. For mechanical drawings of these example retention methods, please see *WP 419 Torpedo SOM Mechanical Hold-Down Scenarios*.

2.3.3 Pick and Place Recommendations

The connectors for the OMAP35x Torpedo SOM can be difficult for standard pick and place machines. Follow the recommendations below to ensure straight connectors during assembly.

- Modify the size of the pick and place nozzle. The correct size for the DS connector is .99 mm.
- Place the nozzle during pick on the indentation in the connector made for the nozzle.
- Slow the horizontal velocity when moving and the rotation speed when making turns. Excessive speeds can cause the connector to slip on the nozzle, placing the connector out of alignment.

2.3.4 Insertion Procedures

The Hirose connector used on the OMAP35x Torpedo SOM is not keyed. Incorrect insertion will damage the SOM. To guarantee correct insertion direction, follow the recommendations below.

- On the baseboard silkscreen, add outlines of the processor and the top side debug connector.
- Add a picture of the correct insertion direction to any technical instructions and post a copy of the picture above workstations where insertion is completed.

3 Electrical Specification

Table 3.1: Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
DC 5V Supply Voltage	5V	0.0 to 7.0	V
DC Main Battery Input Voltage	MAIN_BATTERY	0.0 to 4.5	V
DC USB1 VBUS Input Voltage	USB1_VBUS	0.0 to 7.0	V
RTC Backup Battery Voltage	BACKUP_BATT	0.0 to 3.3	V

NOTE: These stress ratings are only for transient conditions. Operation at, or beyond, absolute maximum rating conditions may affect reliability and cause permanent damage to the Torpedo SOM and its components.

Table 3.2: Recommended Operating Conditions

Parameter	Min	Typical	Max	Unit	Notes
DC Main Battery Input Voltage	**2.7*** (see note 10)	3.3	4.5	V	10
DC Main Battery Active Current, LogicLoader (Main Battery Voltage=4.0V)	—	281	—	mA	7
DC Main Battery Active Current, Windows CE (Main Battery Voltage=4.0V)	—	130	—	mA	8
DC Main Battery Suspend Current, Windows CE (Main Battery Voltage=4.0V)	1.37	86.5	—	mA	9
DC 5V Voltage	4.6	4.6	7.0	V	4, 5, 6
DC USB1_VBUS Input Voltage	4.4	5.0	7.0	V	6
DC RTC Backup Battery Voltage	1.8	3.2	3.3	V	
Commercial Operating Temperature	0	25	70	°C	
Industrial Operating Temperature	-40	25	85	°C	
Storage Temperature	-40	25	85	°C	
Dimensions	—	15.0 x 27.0 x 3.8	—	mm	
Weight	—	2.0	—	Grams	2
Connector Insertion/Removal	—	30	—	Cycles	
Input Signal High Voltage	0.65 x VREF	—	VREF	V	3, 11
Input Signal Low Voltage	-0.3	—	0.35 x VREF	V	3, 11
Output Signal High Voltage	VREF - 0.2	—	VREF	V	3, 11
Output Signal Low Voltage	GND	—	0.2	V	11

TABLE NOTES:

1. General note: CPU power rails are sequenced on the SOM.
2. May vary depending on SOM configuration.

3. VREF represents the peripheral I/O supply reference for the specific CPU voltage rail.

4. Please see Section 5.6.1.2 for detailed information about 5V usage on the OMAP35x Torpedo SOM.

5. The minimum voltage value of the charging device is:

   VBATMAX + 2 PMOS drop + 0.22 ohm resistor drop (where VBATMAX is the maximum voltage value of the battery; that is, 4.2V for Li-ion battery)

6. High input voltage levels may limit the charging capabilities of the SOM. Please reference Logic PD's *AN416 OMAP35x Torpedo SOM Power Management* for more information.

7. Typical current measurement taken on a baseboard and SOM with only RS-232 connected externally; LogicLoader idle (running MD5SUM on the LogicLoader code space in RAM).

8. Typical current measurement taken on a baseboard and SOM with only RS-232 connected externally; Windows CE BSP v2.1.0 idle (at the desktop).

9. Typical current measurement taken on a baseboard and SOM with only RS-232 connected externally; Windows CE BSP v2.1.0 after selecting suspend from start menu. Minimum current measurement taken on a baseboard and SOM using a modified, pre-release Windows CE BSP v2.1.0.

10. 2.7V is the minimum threshold for the battery at which the device will turn OFF. However, the minimum voltage at which the device will power ON is 3.2V ±100mV (if PWRON does not have a switch and is connected to MAIN_BATTERY) considering battery plug as the device switch on event. If PWRON has a switch, then 3.2V is the minimum for the device to turn ON.

11. The exact minimum and maximum values depend on the specific pin being referenced. Please refer to TI's *OMAP3530/25 Applications Processor Datasheet* and *TPS65950 Data Manual* for exact values.

4 Peripheral Specification

4.1 Clocks

The OMAP35x requires an oscillator and crystal to enable proper internal timing. A 26.000 MHz oscillator is used to generate many of the processor's internal clocks via a series of Phase Lock Loops (PLLs) and signal dividers. To generate the core CPU clock, the 26.000 MHz signal is run through a Digital PLL controlled by the PRCM registers. Divisors are used to divide down the internal bus frequency to set the LCD, memory controller, camera interface, etc.

IMPORTANT NOTE: Please see TI's *OMAP35x TRM* for additional information about processor clocking.

The second required crystal runs at 32.768 kHz and is connected directly to the TPS65950. The 32.768 kHz clock is used for PMIC and CPU start up and as a reference clock for the real time clock (RTC) module.

The CPU's microcontroller core clock speed is initialized by software on the OMAP35x Torpedo SOM. The SDRAM bus speed is set at 166 MHz in LogicLoader. Other clock speeds, such as core speed and specific serial baud rates, can be supported and modified in software for specific user applications.

The OMAP35x Torpedo SOM provides an external bus clock, uP_BUS_CLK. This clock is driven by the GPMC_CLK pin.

Table 4.1: Microcontroller Clock Specifications

OMAP35x Microcontroller Signal Name	OMAP35x Torpedo SOM Net Name	Default Software Value in LogicLoader
CORE	N/A	Up to 600 MHz
SDRC_CLK	N/A	166 MHz
GPMC_CLK	uP_BUS_CLK	Not configured

4.2 Memory

4.2.1 Package-on-Package Memory (Mobile DDR and NAND)

The OMAP35x processor uses Package on Package (PoP) technology to stack BGA memory devices on top of the CPU BGA. The OMAP35x uses a 32-bit memory bus to interface to mobile DDR SDRAM and a 16-bit memory bus to interface to NAND. The PoP devices can be ordered with the following density options:

- 128 MB Mobile DDR and 256 MB NAND
- 256 MB Mobile DDR and 512 MB NAND

Logic PD's default memory configuration on the OMAP35x Torpedo SOM included in the Zoom OMAP35x Torpedo Development Kit is specified as 128 MB Mobile DDR and 256 MB NAND.

4.2.2 External Memory

It is possible to expand the system's non-volatile storage capability by adding external flash ICs, SD memory, CompactFlash, or NAND flash. Please contact Logic PD for other possible peripheral designs.

4.3 Audio Codec

The OMAP35x processor has multiple Multi-channel Buffered Serial Port (McBSP) interfaces that support PCM and I2S formats. Both PCM and I2S serial paths drive the built-in TPS65950 audio codec. From the TPS65950, the outputs are CODEC_OUTL and CODEC_OUTR; these signals are available from the expansion connectors.

The codec in the TPS65950 performs up to full-duplex codec functions and supports variable sample rates from 8–96k samples per second. See the "Audio" chapter in TI's *TPS65950 OMAP Power Management TRM* for more information.

NOTE: The OMAP35x Torpedo SOM also offers alternate serial interfaces for other codec devices. If you are looking for a different codec option, Logic PD has previously interfaced different high-performance audio codecs into other SOMs. Contact Logic PD for assistance in selecting an appropriate audio codec for your application.

4.4 Display Interface

The OMAP35x has a built-in LCD controller supporting STN, color STN, and TFT panels at a resolution of up to XGA 1024 x 768 x 24-bit color. See TI's *OMAP35x TRM* for further information on the integrated LCD controller. The signals from the OMAP35x LCD controller are organized by bit and color and can be interfaced through the expansion connectors. Logic PD has written drivers for panels of different types and sizes. Contact Logic PD before selecting a panel for your application.

IMPORTANT NOTE: Using the internal graphics controller will affect processor performance. Selecting display resolutions and color bits per pixel will vary processor busload.

4.5 Serial Interfaces

The OMAP35x Torpedo SOM comes with the following serial channels: UARTA, UARTB, UARTC, three SPI ports, two MCBSP, and two I2C ports. If additional serial channels are required, please contact Logic PD for reference designs. Please see TI's *OMAP35x TRM* for further information regarding serial communications.

4.5.1 UARTA

UARTA has been configured as the main OMAP35x Torpedo SOM serial port based on the processor UART1. It is an asynchronous 16C750-compatible UART. This UART provides a high-speed serial interface that uses 64 byte First In/First Out (FIFO) and is capable of sending and receiving serial data simultaneously. The signals from the OMAP35x Torpedo SOM are 1.8V Transistor-Transistor Logic (TTL) level signals, not RS232 level signals. The end-product design must provide an external RS232 transceiver for RS232 applications. Logic PD has provided an example reference design with the Zoom OMAP35x Torpedo Development Kit.

When choosing an RS232 transceiver, the designer should keep in mind cost, availability, ESD protection, and data rates.

The UARTA baud rate is set to a default 115.2 Kbits/sec, though it supports most common serial baud rates.

4.5.2 UARTB

Serial Port UARTB (processor UART3) is an asynchronous 16C750-compatible UART. This UART is a high-speed serial interface that uses FIFO and is capable of sending and receiving serial data simultaneously. The signals from the OMAP35x Torpedo SOM are 1.8V TTL level signals, not RS232 level signals. The UARTB baud rate can also be set to most common serial baud rates.

4.5.3 UARTC

Serial port UARTC (processor UART2) is an asynchronous 16C750-compatible UART. This UART is a high-speed serial interface that uses FIFO and is capable of sending and receiving serial data simultaneously. The signals from the OMAP35x Torpedo SOM are 1.8V TTL level signals, not RS232 level signals. The UARTC baud rate can also be set to most common serial baud rates.

4.5.4 McSPI

The OMAP35x Torpedo SOM provides three external SPI ports with multiple chip selects. Additional SPI ports are available through different resistor populations. Please see Table 7.1 for more information.

4.5.5 I2C

The OMAP35x Torpedo SOM supports two dedicated external I2C ports. The clock and data signals for the I2C2 port have 4.7K ohm pull-up resistors; the clock and data signals for the I2C3 port have 470 ohm pull-up resistors. Please see TI's *OMAP35x TRM* for further information.

4.5.5.1 Reserved I2C Addresses

The OMAP35x Torpedo SOM contains a product ID chip that connects to the I2C bus. Logic PD software uses this product ID chip to determine hardware version information. As a result, the 7-bit I2C addresses listed below are used by the product ID chip and must be avoided in custom designs:

- 101 1000
- 101 1001
- 101 1010
- 101 1011
- 101 1100
- 101 1101

4.6 USB Interface

The OMAP35x Torpedo SOM supports one USB 2.0 OTG port, which can function as a host or device/client. In order to for the port to operate as a host, a proper adapter cable must be used; Logic PD recommends one similar to the USB adapter cable by Digi-Key[12] (part number 10-00003-ND). The port can operate at up to 480 Mbit/sec. The processor has the USB controller internal to the OMAP for the OTG port; an external PHY built into the TPS65950 supports the OTG port. For more information on using the OTG interfaces, please see TI's *OMAP35x TRM*.

IMPORTANT NOTE: In order to correctly implement USB on the OMAP35x Torpedo SOM, additional impedance matching circuitry may be required on the USB1_D+ and USB1_D- signals before they can be used. USB 2.0 requirements specify the signals must be routed as differential pairs with 90 ohm differential impedance. Refer to the *USB 2.0 Specification* for detailed information.

4.7 General Purpose I/O

Logic PD designed the OMAP35x Torpedo SOM to be flexible and provide multiple options for analog and digital GPIO. There are numerous digital GPIO pins on the SOM that interface to the OMAP35x processor and TPS65950 PMIC; see Section 7 for more information. If certain peripherals are not desired, such as the LCD controller, chip selects, IRQs, or UARTs, then more GPIO pins become available.

DESIGN NOTE: Due to buffer strength, an external serial resistor must be connected to the BGA balls where GPIO_120 through GPIO_129 are muxed with MMC signals. See "Section 24.2" in TI's *OMAP35x TRM* for additional information.

4.8 Expansion/Feature Options

The OMAP35x Torpedo SOM was designed for expansion and a variable feature set, providing all the necessary control signals and bus signals to expand the user's design. Some of these signals are buffered and brought out to the expansion connectors. It is possible for a user to expand the SOM's functionality even further by adding host bus or ISA bus devices. Some features that are implemented on the OMAP35x, but are not discussed herein, include: RTC, pulse width modulation (PWM), Secure Digital, MMC cards, SDIO cards, graphics accelerator, DSP codecs, Image Processing Unit, 1-wire interface, and the debug module. See TI's *OMAP35x TRM* and Logic PD's *Torpedo SOM Schematics* for more details. Logic PD has experience implementing additional options, including other audio codecs, Ethernet ICs, co-processors, and components on SOMs. Contact Logic PD for potential reference designs before selecting your peripherals.

DESIGN NOTE: Due to buffer strength, an external serial resistor must be connected to the BGA balls corresponding to any MMC/SD1 signal or alternate function on those same BGA balls. See "Section 24.2" in TI's *OMAP35x TRM* for additional information.

[12] http://www.digikey.com/scripts/DkSearch/dksus.dll?WT.z_header=search_go&lang=en&keywords=10-00003-ND&x=0&y=0&cur=USD

5 System Integration

5.1 Configuration

The OMAP35x Torpedo SOM was designed to meet multiple applications for users with specific design and budget requirements. As a result, this SOM supports a variety of embedded operating systems and hardware configurations. Please contact Logic PD for additional hardware configurations to meet your application needs.

5.2 Resets

The OMAP35x Torpedo SOM has a reset input (MSTR_nRST) and a reset output (SYS_nRESWARM). External devices can drive MSTR_nRST low to assert reset to the product. The OMAP35x Torpedo SOM uses SYS_nRESWARM to indicate to other devices that the SOM is in reset.

5.2.1 Master Reset (MSTR_nRST)—Reset Input

Logic PD suggests that custom designs implementing the OMAP35x Torpedo SOM use the MSTR_nRST signal as the “pin-hole” reset used in commercial embedded systems. The MSTR_nRST triggers a power-on-reset event to the OMAP35x processor and resets the entire CPU.

IMPORTANT NOTE: MSTR_nRST does not reset the TPS65950; the TPS65950 is only reset by removing power from the SOM.

IMPORTANT NOTE: Any custom reset circuit design should guard the assertion of the reset lines during a low power state so as to prevent power-up in a low or bad power condition. Powering up in a low or bad power condition will cause data corruption and, possibly, temporary system lockup; see Section 5.6 for further details. Either one of the following two conditions will cause a system-wide reset: power on the MSTR_nRST signal or a low pulse on the MSTR_nRST signal.

Low Pulse on MSTR_nRST Signal:

A low pulse on the MSTR_nRST signal, asserted by an external source (for example, the reset button on the custom design application) will bring MSTR_nRST low until the assertion source is de-asserted. There is no delay beyond the de-assertion of the external MSTR_nRST signal source, so the custom design must ensure that the assertion time is sufficient for all related peripherals.

Logic PD suggests using de-bouncing to generate a clean, one-shot reset signal for any external assertion source that triggers the MSTR_nRST signal, analog or digital.

5.2.2 Torpedo SOM Reset (SYS_nRESWARM)—Reset output

All hardware peripherals should connect their hardware-reset pin to the SYS_nRESWARM signal on the expansion connector. Internally, all OMAP35x Torpedo SOM peripheral hardware reset pins are connected to the SYS_nRESWARM net.

5.3 Interrupts

The OMAP35x incorporates the ARM Cortex-A8 interrupt controller, which provides many inter-system interrupt sources and destinations. Most external GPIO signals can also be configured as interrupt inputs by configuring their pin control registers. Logic PD BSPs set up and process all onboard system and external OMAP35x Torpedo SOM interrupt sources. Refer to TI's *OMAP35x TRM* for further information on using interrupts.

5.4 JTAG Debugger Interface

The JTAG connection on the OMAP35x allows recovery of corrupted flash memory, real-time application debug, and DSP development. There are several third-party JTAG debuggers available for TI microcontrollers. The following signals make up the JTAG interface to the OMAP35x processor: TDI, TMS, TCK, TDO, nTRST, RTCK, EMU0, and EMU1. These signals are routed to reference designator J5 on the SOM.

IMPORTANT NOTE: When laying out the 20-pin connector, realize that it may not be numbered as a standard 20-pin 0.1" insulation displacement connector (IDC) through-hole connector. See the Embedded Trace Macrocell (ETM) Adapter Board reference design for further details. Each JTAG tool vendor may define the 20-pin IDC connector pin-out differently.

5.5 ETM Adapter Interface

The ETM interface signals are available through connector J5 on the OMAP35x Torpedo SOM. Logic PD developed an adapter board included with the Zoom OMAP35x Torpedo Development Kit that converts the available signals on J5 to the standard Mictor connector interface used by most common third-party ETM tool providers. The connector supports ETM_D[15:0], ETM_CLK, ETM_CTL, and the JTAG signals listed in Section 5.4.

5.6 Power Management

5.6.1 System Power Supplies

In order to ensure a flexible design, the OMAP35x Torpedo SOM has the following power areas: MAIN_BATTERY, 5V, USB1_VBUS, and BACKUP_BATT. All power areas are inputs to the SOM. The module also provides VIO_1V8 as a reference voltage. It may be used to supply up to 200 mA of power, but it is recommended to use an external supply.

5.6.1.1 MAIN_BATTERY

The MAIN_BATTERY input is the main source of power for the OMAP35x Torpedo SOM. This input expects a voltage within typical single lithium-ion battery limits which generally operate from 2.7V to 4.2V. If a lithium-ion battery is not used as the main power source, it is

recommended to supply a fixed 3.3V supply. The TPS65950 power management controller takes the MAIN_BATTERY rail input and creates all onboard voltages. If the design is required to maintain RAM contents in a critical power situation (e.g., low battery, loss of power), the MAIN_BATTERY supply should be maintained above the minimum level at all costs (see Section 2). Logic PD suggests using the standby mode to prepare the system for a critical power condition. In this way, the SDRAM is placed into self-refresh and the processor is placed into the standby state. (Please note the description of standby mode in Section 5.6.3.3 below.) The MAIN_BATTERY supply must stay within the acceptable levels specified in Section 2 unless experiencing power-down or critical power conditions.

5.6.1.2 5V

The 5V input is not required for product operation. The 5V input is only used to provide a charge to the MAIN_BATTERY rail on the OMAP35x Torpedo SOM. The charge path circuit allows in-system charging of a single cell lithium-ion battery source when power is applied to the 5V supply. Charge current is limited based on input voltage and operating temperature; please see Logic PD's *AN 416 OMAP35x Torpedo SOM Power Management* for details on charging capabilities. Some designs will require a separate battery charging circuit on the baseboard to charge the main battery source.

NOTE: While charging, 5V will also power the SOM if it is left in an active state; therefore, the charging current will be minus the system operating current.

5.6.1.3 USB1_VBUS

If the OMAP35x Torpedo SOM is connected to a USB host, USB1_VBUS can be used to charge MAIN_BATTERY. USB charging is disabled by default, but can be enabled through software. Please refer to TI's *TPS65950 OMAP Power Management TRM* document for more information. Charge current is limited based on input voltage and operating temperature; please see Logic PD's *AN416 OMAP35x Torpedo SOM Power Management* for details on charging capabilities. Some designs will require a separate battery charging circuit on the baseboard to charge the main battery source.

NOTE: While charging, USB1_VBUS will also power the SOM if it is left in an active state; therefore, the charging current will be minus the system operating current.

5.6.1.4 BACKUP_BATT

The BACKUP_BATT power rail is used to power the onboard TPS65950, power management state machine, and RTC circuit when MAIN_BATTERY is not present. Always power this rail to maintain the clock and power state of the product. A lithium-ion coin cell typically supplies power to this rail. The TPS65950 overrides this input when MAIN_BATTERY is applied.

5.6.2 System Power Management

Good power management design is important in any system development and embedded system design is no exception. In embedded system design, power management is typically one of the most complicated areas due to the dramatic effect it has on product cost, performance, usability, and overall customer satisfaction. Many factors affect a power-efficient hardware design: power supply selection (efficiency), clocking design, IC and component selection, etc. The OMAP35x Torpedo SOM was designed with these aspects in mind while also providing maximum flexibility in software and system integration.

On the OMAP35x there are many different software configurations that drastically affect power consumption: microcontroller core clock frequency, bus clock frequency, peripheral clocks, bus modes, power management states; peripheral power states and modes; product user scenarios; interrupt handling; and display settings (resolution, backlight, refresh, bits per pixel, etc). These settings are typically initialized in the startup software routines and may be modified later in the operating system and application software. Information for these items can be found in the appropriate documents, such as the *LogicLoader v2.4 User Manual* or the specific BSP manual.

5.6.2.1 T2_REGEN

T2_REGEN is an open drain output from the TPS65950. It can be used to control power for external power ICs or LDOs. Please see the *TPS65950 OMAP Power Management TRM* for more information.

5.6.3 Microcontroller

The OMAP35x processor's power management scheme was designed for the cellular handset market, which means the static and dynamic power consumption has very flexible controls allowing designers to tweak the processor to minimize end-product power consumption. Logic PD software BSPs take advantage of Dynamic Power Switching and SmartReflex Adaptive Voltage Control to maximize power savings.

5.6.3.1 Run State

Run is the normal operating state for the OMAP35x Torpedo SOM in which oscillator outputs and all clocks are hardware enabled. The OMAP35x can enter run mode from any state. A standby-to-run transition occurs on any valid wakeup event, such as the assertion or any enabled interrupt signal. All required power supplies are active in this state. Please see TI's *OMAP35x TRM* for further information.

5.6.3.2 Suspend State

Suspend is the hardware power-down state for the OMAP35x Torpedo SOM, allowing for lower power consumption. The suspend state is designed to reduce power consumption while the OMAP35x is waiting for an event, such as a keyboard input. In Logic PD BSPs, the suspend state is entered through software commands. All power supplies remain active and system context is retained. An internal or external wakeup event can cause the processor to transition back to run mode. Please see TI's *OMAP35x TRM* for further information.

5.6.3.3 Standby State

Standby is the lowest power state for the OMAP35x Torpedo SOM. This state is entered in Logic PD BSPs through software commands. The OMAP35x processor is put into the lowest power state and all clocks are stopped. The MAIN_BATTERY power rail should be maintained if the low-power DDR SDRAM contents wish to be retained. Internal or external wakeup events can cause a return to the run state.

5.7 Boot Modes

The OMAP35x provides the option of booting from multiple sources. The boot mode is controlled by the SYS_BOOT pins of the processor. SYS_BOOT0 and SYS_BOOT5 are available off-board through the expansion connectors. Please see TI's *OMAP35x TRM* for further information. The available boot options are shown in Table 5.1 below.

Table 5.1: Signals for Multiple Boot Sources

OMAP35x Processor Pins	Boot Method
Default SYS_BOOT[6:0] =1101111	USB, UART3, MMC1, NAND
Alternate SYS_BOOT[6:0] =1001111	NAND, USB, UART3, MMC1
Alternate SYS_BOOT[6:0] =1001110	XIPwait, DOC, USB, UART3, MMC1
Alternate SYS_BOOT[6:0] =1000110	MMC1 USB

5.8 ESD Considerations

The OMAP35x Torpedo SOM was designed to interface to a customer's peripheral board, while remaining low cost and adaptable to many different applications. The OMAP35x Torpedo SOM does not provide any onboard ESD protection circuitry—this must be provided by the product it is used in. Logic PD has extensive experience in designing products with ESD requirements. Please contact Logic PD if you need any assistance in ESD design considerations.

6 Memory & I/O Mapping

On the OMAP35x microcontroller, all address mapping for the GPMC chip select signals is listed below. Mapped "chip select" signals for the OMAP are available as outputs from the microcontroller and are assigned as described in Table 6.1 below.

Table 6.1: Chip Select Signals

Chip Select	Device/Feature	Notes
nCS0	POP NAND	Boot chip select for PoP NAND device
nCS1	uP_nCS1	Available for use by an off-board external device
nCS2	uP_nCS2	Available for use by an off-board external device
nCS3	uP_nCS3	Available for use by an off-board external device
nCS4	uP_nCS4	Available for use by an off-board external device
nCS5	uP_nCS5	Available for use by an off-board external device
nCS6	uP_nCS6	Available for use by an off-board external device

NOTE: Memory addresses for chip selects on the OMAP35x are configurable by software; therefore, precise address locations cannot be provided. Please consult the *LogicLoader v2.4 User Manual* and the *OMAP35x Torpedo SOM LogicLoader User Manual Addendum* for memory map information.

7 Pin Descriptions & Functions

IMPORTANT NOTE: The following pin descriptions and states are provided for the default pin usage. Many of the signals defined in the connector tables can be configured as input or outputs—most GPIOs on the OMAP35x processor can be configured as either inputs or outputs—and have different functions. It is critical to review all signals in the final design (both electrical and software) to verify the necessary configuration (external pull-ups/pull-downs).

IMPORTANT NOTE: Please pay special attention to the reference voltage of the OMAP35x used to power each signal in the table below, especially when used as a GPIO. Not all power rails coming out of the TPS65950 are on by default and may need to be enabled through software. Reference voltages for OMAP35x signals can be found in "Table 2-1" of TI's *OMAP3530/25 Applications Processor Datasheet*.

7.1 J1 Connector 100-Pin Descriptions

J1 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J1.1	uP_nWE	F4	GPMC_nWE	O	1.8V	Low indicates processor is writing. High indicates processor is reading. (See notes 1 & 2)
J1.2	CODEC_OUTL	B4 (PMIC)	HSOL (PMIC)	O	max 2.7V	Left channel headset out.
J1.3	VMMC1	C2 (PMIC) K25	VMMC1.OUT (PMIC) VDDS_MMC1	O	3.0V (configurable)	MMC/SD1 interface voltage reference output.
J1.4	CODEC_INR	G1 (PMIC)	AUXR (PMIC)	I	max 2.7V	Auxiliary right channel line in.
J1.5	PWRON	A11(PMIC)	PWRON (PMIC)	I	Max 4.5V (MAIN_BATTERY)	Active low. Software can use this signal as an interrupt to transition to RUN state from lower power states. Software is required for proper operation. This signal has a 4.75K pull up.
J1.6	CODEC_INL	F1 (PMIC)	AUXL (PMIC)	I	max 2.7V	Auxiliary left channel line in.
J1.7	uP_A9	L3	GPMC_A9/ SYS_nDMAREQ2/ GPIO_42	O	1.8V	Processor GPMC bus address bit 9.
J1.8	MIC_IN	E3 (PMIC) E4 (PMIC)	HSMIC.P (PMIC) VHSMI.OUT (PMIC)	I	max 2.7V	Microphone input.
J1.9	uP_nCS0	G4	GPMC_nCS0	O	1.8V	uP_nCS0 is used by the PoP NAND Flash device. This signal MUST be left unconnected, unless the PoP chip does not contain NAND. (See note 1)
J1.10	CODEC_OUTR	B5 (PMIC)	HSOR (PMIC)	O	max 2.7V	Right channel headset out.
J1.11	uP_nCS1	H3	GPMC_nCS1/ GPIO_52	O	1.8V	External Chip select available for customer use.
J1.12	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.

J1 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J1.13	uP_A8	M3	GPMC_A8/GPIO_41	O	1.8V	Processor GPMC bus address bit 8.
J1.14	MAIN_BATTERY	(See Schematic)	(See Schematic)	I	max 4.5V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed 3.3V regulated power source.
J1.15	uP_nOE	G2	GPMC_nOE	O	1.8V	Active low. Used to indicate processor is reading from external devices. (See notes 1 & 2)
J1.16	MAIN_BATTERY	(See Schematic)	(See Schematic)	I	max 4.5V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed 3.3V regulated power source.
J1.17	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J1.18	MAIN_BATTERY	(See Schematic)	(See Schematic)	I	max 4.5V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed 3.3V regulated power source.
J1.19	uP_BUS_CLK	T4	GPMC_CLK/ GPIO_59	O	1.8V	Processor bus clock. Frequency varies based on software setup. Note: uP_BUS_CLK is only active on bus transactions, it does not run continuously. See TI's OMAP35xx TRM and Data Sheet for additional information.
J1.20	MAIN_BATTERY	(See Schematic)	(See Schematic)	I	max 4.5V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed 3.3V regulated power source.
J1.21	uP_nBE1	U3	GPMC_nBE1/ GPIO_61	O	1.8V	Processor bus Byte Lane Enable 1 bits [15:8]
J1.22	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J1.23	uP_nADV_ALE	F3	GPMC_nADV_ALE	O	1.8V	Processor GPMC address valid or address latch enable signal. (See notes 1 & 2)
J1.24	BACKUP_BATT	M14(PMIC)	BKBAT (PMIC)	I	1.8V-3.3V	External input that supplies power to the onboard power management controller and RTC interface. This signal should be powered by a coin-cell type battery or an always-on power source.
J1.25	uP_nBE0	G3	GPMC_nBE0_CLE/ GPIO_60	O	1.8V	Processor bus Byte Lane Enable 0 bits [7:0]. Also functions as CLE for NAND Flash. (See notes 1 & 2)

J1 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J1.26	uP_nWAIT	M8	GPMC_WAIT0	I	1.8V	Active low. Processor bus GPMC_WAIT0 signal. Used to extend bus transactions beyond programmed wait states. The external device signals completion of the cycle by deasserting the uP_nWAIT signal. This signal is connected to the POP NAND Flash R/B signal. (See notes 1 & 2)
J1.27	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J1.28	uP_nCS6	P8	GPMC_nCS6/ SYS_nDMAREQ3/ McBSP4_DX/ GPT11_PWM_EVT/GP IO_57	O	1.8V	External Chip select available for customer use.
J1.29	uP_D8	H2	GPMC_D8/GPIO_44	I/O	1.8V	Processor GPMC bus data bit 8. (See notes 1 & 2)
J1.30	uP_DREQ0	J8	GPMC_WAIT3/ SYS_nDMAREQ1/ GPIO_65	I	1.8V	DMA Request signal for DMA4. Connected to SYS_nDMAREQ1 of the OMAP35x. Note: This signal is shared with the POP NAND chip's LOCK pin. This signal must be left floating at power-on to avoid conflict.
J1.31	uP_D9	K2	GPMC_D9/GPIO_45	I/O	1.8V	Processor GPMC bus data bit 9. (See notes 1 & 2)
J1.32	uP_nCS5	R8	GPMC_nCS5/ SYS_nDMAREQ2/ McBSP4_DR/ GPT10_PWM_EVT/ GPIO_56	O	1.8V	External Chip select available for customer use.
J1.33	uP_D2	L2	GPMC_D2	I/O	1.8V	Processor GPMC bus data bit 2. (See notes 1 & 2)
J1.34	uP_nCS4	T8	GPMC_nCS4/ SYS_nDMAREQ1/ McBSP4_CLKX/ GPT9_PWM_EVT/ GPIO_55	O	1.8V	External Chip select available for customer use.
J1.35	uP_D0	K1	GPMC_D0	I/O	1.8V	Processor GPMC bus data bit 0. (See notes 1 & 2)
J1.36	uP_nCS3	U8	GPMC_nCS3/ SYS_nDMAREQ0/ GPIO_54	O	1.8V	External Chip select available for customer use.
J1.37	uP_D1	L1	GPMC_D1	I/O	1.8V	Processor GPMC bus data bit 1. (See notes 1 & 2)
J1.38	uP_A10	K3	GPMC_A10/ SYS_nDMAREQ3/ GPIO_43	O	1.8V	Processor GPMC bus address bit 10.
J1.39	uP_D3	P2	GPMC_D3	I/O	1.8V	Processor GPMC bus data bit 3. (See notes 1 & 2)

J1 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J1.40	uP_nCS2	V8	GPMC_nCS2/ GPIO_53	O	1.8V	External Chip select available for customer use.
J1.41	uP_D12	R2	GPMC_D12/ GPIO_48	I/O	1.8V	Processor GPMC bus data bit 12. (See notes 1 & 2)
J1.42	uP_A4	K4	GPMC_A4/GPIO_37	O	1.8V	Processor GPMC bus address bit 4.
J1.43	uP_D10	P1	GPMC_D10/ GPIO_46	I/O	1.8V	Processor GPMC bus data bit 10. (See notes 1 & 2)
J1.44	uP_A3	L4	GPMC_A3/GPIO_36	O	1.8V	Processor GPMC bus address bit 3.
J1.45	uP_D11	R1	GPMC_D11/ GPIO_47	I/O	1.8V	Processor GPMC bus data bit 11. (See notes 1 & 2)
J1.46	uP_A2	M4	GPMC_A2/GPIO_35	O	1.8V	Processor GPMC bus address bit 2.
J1.47	uP_D13	T2	GPMC_D13/ GPIO_49	I/O	1.8V	Processor GPMC bus data bit 13. (See notes 1 & 2)
J1.48	uP_A1	N4	GPMC_A1/GPIO_34	O	1.8V	Processor GPMC bus address bit 1.
J1.49	uP_D4	T1	GPMC_D4	I/O	1.8V	Processor GPMC bus data bit 4. (See notes 1 & 2)
J1.50	uP_A7	N3	GPMC_A7/GPIO_40	O	1.8V	Processor GPMC bus address bit 7.
J1.51	MCSPI2_CS1	V3	McSPI2_CS1/ GPT8_PWM_EVT/ HSUSB2_TLL_DATA3/ USUSB2_DATA3/ MM2_TXEN_N/ GPIO_182	O	1.8V	McSPI2 interface chip select 1 output.
J1.52	uP_A6	R3	GPMC_A6/GPIO_39	O	1.8V	Processor GPMC bus address bit 6.
J1.53	uP_D6	V2	GPMC_D6	I/O	1.8V	Processor GPMC bus data bit 6. (See notes 1 & 2)
J1.54	uP_A5	T3	GPMC_A5/GPIO_38	O	1.8V	Processor GPMC bus address bit 5.
J1.55	uP_D7	W2	GPMC_D7	I/O	1.8V	Processor GPMC bus data bit 7. (See notes 1 & 2)
J1.56	MCSPI2_SOMI	Y3	McSPI2_SOMI/ GPT10_PWM_EVT/ HSUSB2_TLL_DATA5/ HSUSB2_DATA5/ GPIO_180	I	1.8V	McSPI2 interface receive input.
J1.57	uP_D5	V1	GPMC_D5	I/O	1.8V	Processor GPMC bus data bit 5. (See notes 1 & 2)
J1.58	MCSPI2_CS0	Y4	McSPI2_CS0/ GPT11_PWM_EVT/ HSUSB2_TLL_DATA6/ HSUSB2_DATA6/ GPIO_181	O	1.8V	McSPI2 interface chip select 0 output.
J1.59	uP_D14	W1	GPMC_D14/GPIO_50	I/O	1.8V	Processor GPMC bus data bit 14. (See notes 1 & 2)

J1 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J1.60	MCSPI1_SOMI	AA4	McSPI1_SOMI/ MMC2_DAT6/ GPIO_173	I	1.8V	McSPI1 interface receive input.
J1.61	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J1.62	MCBSP4_DR	AD1	McBSP4_DR/ SSI1_FLAG_RX/ HSUSB3_TLL_DATA0/ MM3_RXRCV/ GPIO_153	I	1.8V	McBSP4 interface receive input.
J1.63	uP_D15	Y1	GPMC_D15/GPIO_51	I/O	1.8V	Processor GPMC bus data bit 15. (See notes 1 & 2)
J1.64	MCSPI1_CLK	AB3	McSPI1_CLK/ MMC2_DAT4/ GPIO_171	O	1.8V	McSPI1 serial clock signal.
J1.65	MCSPI2_SIMO	Y2	McSPI2_SIMO/ GPT9_PWM_EVT/ HSUSB2_TLL_DATA4/ HSUSB2_DATA4/ GPIO_179	O	1.8V	McSPI2 interface transmit output.
J1.66	MCSPI1_SIMO	AB4	McSPI1_SIMO/ MMC2_DAT5/ GPIO_172	O	1.8V	McSPI1 interface transmit output.
J1.67	MCSPI2_CLK	AA3	McSPI2_CLK/ HSUSB2_TLL_DATA7/ HSUSB2_DATA7/ GPIO_178	O	1.8V	McSPI2 serial clock signal.
J1.68	uP_UARTA_CTS	W8	UART1_CTS/ SSI1_RDY_TX/ HSUSB3_TLL_CLK/ GPIO_150	I	1.8V	Clear To Send signal for UART1.
J1.69	MCSPI1_CS1	AC3	McSPI1_CS1/ ADPLLV2D_ DITHERING_EN2/ MMC3_CMD/ GPIO_175	O	1.8V	McSPI1 interface chip select 1 output.
J1.70	uP_UARTA_RX	Y8	UART1_RX/ MCBSP1_CLKR/ MCSPI4_CLK/ GPIO_151	I	1.8V	Data Receive signal for UART1.
J1.71	MCSPI1_CS0	AC2	McSPI1_CS0/ MMC2_DAT7/ GPIO_174	O	1.8V	McSPI1 interface chip select 0 output.
J1.72	uP_UARTA_TX	AA8	UART1_TX/ SSI1_DAT_TX/ GPIO_148	O	1.8V	Data Transmit signal for UART1.
J1.73	LCD_PANEL_PWR	AC1	McBSP4_FSX/ SSI1_WAKE/ HSUSB3_TLL_DATA3/ MM3_TXEN_n/ GPIO_155	O	1.8V	LCD Panel Power signal.

J1 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J1.74	uP_UARTA_RTS	AA9	UART1_RTS/ SSI1_FLAG_TX/ GPIO_149	O	1.8V	Ready To Send signal for UART1.
J1.75	LCD_BACKLIGHT_PWR	AD2	McBSP4_DX/ SSI1_RDY_RX/ HSUSB3_TLL_DATA2/ MM3_TXDAT/ GPIO_154	O	1.8V	LCD Backlight Power signal. Active High.
J1.76	R90 Populated **(default)**: ADCIN0 (CONFIG11)	H4 (PMIC)	ADCIN0 (PMIC)	I	max 1.5V	Analog to digital converter input. Connected to TPS65950 ADCIN0.
	R91 Populated: CSI_D8 (CONFIG11)	K27	CAM_D8/GPIO_107	I	1.8V	Camera Sensor Interface Data bit 8.
J1.77	MCBSP3_DR	T15(PMIC) AE6	PCM.VDX (PMIC) McBSP3_DR/ UART2_RTS/ HSUSB3_TLL_DATA5/ GPIO_141	I	1.8V	McBSP3 interface receive input.
J1.78	R90 Populated **(default)**: ADCIN1 (CONFIG10)	J3(PMIC)	ADCIN1 (PMIC)	I	max 1.5V	Analog to digital converter input. Connected to TPS65950 ADCIN1.
	R91 Populated: CSI_D9 (CONFIG10)	L27	CAM_D9/GPIO_108	I	1.8V	Camera Sensor Interface Data bit 9.
J1.79	MCBSP3_DX	T2 (PMIC) AF6	PCM.VDR (PMIC) McBSP3_DX/ UART21_CTS/ HSUSB3_TLL_DATA4/ GPIO_140	O	1.8V	McBSP3 interface transmit output.
J1.80	R90 Populated **(default)**: ADCIN2 (CONFIG9)	G3 (PMIC)	ADCIN2 (PMIC)	I	max 2.5V	Analog to digital converter input. Connected to TPS65950 ADCIN2.
	R91 Populated: CSI_D10 (CONFIG9)	B25	CAM_D10/ SSI2_WAKE/GPIO_109	I	1.8V	Camera Sensor Interface Data bit 10.
J1.81	MCBSP3_FSX	R16(PMIC) AE5	PCM.VFS (PMIC) McBSP3_FSX/ UART2_RX/ HSUSB3_TLL_DATA7/ GPIO_143	I/O	1.8V	McBSP3 transmit frame synchronization.
J1.82	R90 Populated **(default)**: ADCIN3 (CONFIG8)	P11(PMIC)	ADCIN3 (PMIC)	I	max 2.5V	Analog to digital converter input. Connected to TPS65950 ADCIN3.
	R91 Populated: CSI_D11 (CONFIG8)	C26	CAM_D11/GPIO_110	I	1.8V	Camera Sensor Interface Data bit 11.

J1 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J1.83	MCBSP3_CLKX	R1 (PMIC) AF5	PCM.VCK (PMIC) McBSP3_CLKX/ UART2_TX/ HSUSB3_TLL_DATA6/ GPIO_142	O	1.8V	McBSP3 transmit clock output.
J1.84	SD2_DATA0	AH5	MMC2_DAT0/ McSPI3_SOMI/ GPIO_132	I/O	1.8V	MMC/SD2 Data 0 signal. This signal requires a 10K pull-up to VIO_1V8.
J1.85	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J1.86	R86 Populated: LCD_D17 (CONFIG1)	H27	DSS_D17/GPIO_87	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the *OMAP35x TRM* for LCD bus mapping.
	R87 Populated **(default)**: MCSPI1_CS2 (CONFIG1)	AB1	McSPI1_CS2/ MMC3_CLK/ GPIO_176	O	1.8V	McSPI1 interface chip select 2 output.
J1.87	R86 Populated: LCD_D23 (CONFIG2)	AC28	DSS_D23/ SDI_CLKN/ GPIO_93	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the *OMAP35x TRM* for LCD bus mapping.
	R87 Populated **(default)**: SD3_CLK (CONFIG2)	AF10	ETK_CLK/ McBSP5_CLKX/ MMC3_CLK/ HSUSB1_STP/ MM1_RXDP/ HSUSB1_TLL_STP/ GPIO_12	O	1.8V	MMC/SD3 Clock signal. This signal requires a 10K pull-up to VIO_1V8.
J1.88	R86 Populated: MCSPI3_CLK (CONFIG3)	AE13	ETK_D3/McSPI3_CLK / MMC3_DAT3/ HSUSB1_DATA7/ HSUSB1_TLL_DATA7/ GPIO_17	O	1.8V	McSPI3 serial clock signal.
	R87 Populated **(default)**: MCSPI1_CS3 (CONFIG3)	AB2	McSPI1_CS3/ HSUSB2_TLL_DATA2/ MM2_TXDAT/ GPIO_177	O	1.8V	McSPI1 interface chip select 3 output.
J1.89	SD2_CLK	AE2	MMC2_CLK/ McSPI3_CLK/ GPIO_130	O	1.8V	MMC/SD2 Clock signal. This signal requires a 10K pull-up to VIO_1V8.
J1.90	R96 Populated **(default)**: SD3_DATA3 (CONFIG23)	AE3	MMC2_DAT7/ MMC2_CLKIN/ MMC3_DAT3/ HSUSB3_TLL_NXT/ MM3_RXDM/ GPIO_139	I/O	1.8V	MMC/SD3 Data 3 signal. This signal requires a 10K pull-up to VIO_1V8.
	R97 Populated: MCSPI3_SOMI (CONFIG23)	AG12	ETK_D1/ McSPI3_SOMI/ HSUSB1_DATA1/ MM1_TXSE0/ HSUSB1_TLL_DATA1/ GPIO_15	I	1.8V	McSPI3 interface receive input.

J1 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J1.91	SD2_DATA3	AF4	MMC2_DAT3/ McSPI3_CS0/ GPIO_135	I/O	1.8V	MMC/SD2 Data 3 signal. This signal requires a 10K pull-up to VIO_1V8.
J1.92	R96 Populated **(default)**: SD3_DATA2 (CONFIG22)	AF3	MMC2_DAT6/ MMC2_DIR_CMD/ CAM_SHUTTER/ MMC3_DAT2/ HSUSB3_TLL_DIR/ GPIO_138	I/O	1.8V	MMC/SD3 Data 2 signal. This signal requires a 10K pull-up to VIO_1V8.
	R97 Populated: MCSPI3_SIMO (CONFIG22)	AF11	ETK_D0/ McSPI3_SIMO/ MMC3_DAT4/ HSUSB1_DATA0/ MM1_RXRCV/ HSUSB1_TLL_DATA0/ GPIO_14	O	1.8V	McSPI3 interface transmit output.
J1.93	SD2_DATA2	AG4	MMC2_DAT2/ McSPI3_CS1/ GPIO_134	I/O	1.8V	MMC/SD2 Data 2 signal. This signal requires a 10K pull-up to VIO_1V8.
J1.94	R96 Populated **(default)**: SD3_DATA1 (CONFIG21)	AH3	MMC2_DAT5/ MMC2_DIR_DAT1/ CAM_GLOBAL_RESET / MMC3_DAT1/ HSUSB3_TLL_STP/ MM3_RXDP/GPIO_137	I/O	1.8V	MMC/SD3 Data 1 signal. This signal requires a 10K pull-up to VIO_1V8.
	R97 Populated: MCSPI3_CS0 (CONFIG21)	AH12	ETK_D2/McSPI3_CS0 / HSUSB1_DATA2/ MM1_TXDAT/ HSUSB1_TLL_DATA2/ GPIO_16	O	1.8V	McSPI3 interface chip select 0 output.
J1.95	SD2_DATA1	AH4	MMC2_DAT1/GPIO_133	I/O	1.8V	MMC/SD2 Data 1 signal. This signal requires a 10K pull-up to VIO_1V8.
J1.96	R96 Populated **(default)**: SD3_DATA0 (CONFIG20)	AE4	MMC2_DAT4/ MMC2_DIR_DAT0/ MMC3_DAT0/GPIO_136	I/O	1.8V	MMC/SD3 Data 0 signal. This signal requires a 10K pull-up to VIO_1V8.
	R97 Populated: MCSPI3_CS1 (CONFIG20)	AH14	ETK_D7/ McSPI3_CS1/ MMC3_DAT7/ HSUSB1_DATA3/ MM1_TXEN_n/ HSUSB1_TLL_DATA3/ GPIO_21	O	1.8V	McSPI3 interface chip select 1 output.
J1.97	SD2_CMD	AG5	MMC2_CMD/ McSPI3_SIMO/ GPIO_131	I/O	1.8V	MMC/SD2 Command signal. This signal requires a 10K pull-up to VIO_1V8.

J1 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J1.98	uP_IODIR	N8	GPMC_nCS7/ GPMC_IODIR/ McBSP4_FSX/ GPT8_PWM_EVT/ GPIO_58	O	1.8V	When high, external buffers should drive data from external devices towards the Torpedo SOM. (Torpedo SOM is reading) When low, external buffers should drive data from the Torpedo SOM towards external devices. (Torpedo SOM is writing).
J1.99	R86 Populated: LCD_D16 (CONFIG0)	G25	DSS_D16/GPIO_86	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the *OMAP35x TRM* for LCD bus mapping.
	R87 Populated **(default)**: SD3_CMD (CONFIG0)	AE10	ETK_CTL/ MMC3_CMD/ HSUSB1_CLK/ HSUSB1_TLL_CLK/ GPIO_13	O	1.8V	MMC/SD3 Command signal. This signal requires a 10K pull-up to VIO_1V8.
J1.100	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.

TABLE NOTES:

1. Caution must be used when considering these signals for alternative functions as they may connect to the top PoP BGA footprint.

2. When using PoP memories with 16-bit NAND memory, these signals present an additional load on the GPMC bus which must be accounted for when calculating overall bus load.

7.2 J2 Connector 100-Pin Descriptions

J2 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J2.1	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J2.2	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J2.3	USB1_D+	T10(PMIC)	DP/UART3.RXD (PMIC)	I/O	Variable (see note 1)	USB OTG port 1 I/O data plus signal. Route as differential pair with USB1_D-. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differential impedance.
J2.4	VIO_1V8	(See Schematic)	(See Schematic)	O	1.8V	Voltage reference output created on Torpedo.
J2.5	USB1_D-	T11(PMIC)	DN/UART3.TXD (PMIC)	I/O	Variable (see note 1)	USB OTG port 1 I/O data minus signal. Route as differential pair with USB1_D+. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differential impedance.

J2 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J2.6	SYS_nRESWARM	AG13 AF24 B13(PMIC)	POP_RESET_RP_FT SYS_nRESWARM/ GPIO_30 NRESWARM (PMIC)	O	1.8V	Active low. Reset output from the CPU that drives all onboard reset inputs. This signal should be used to drive reset inputs on external chips that require similar timing to the onboard devices. The SYS_nRESWARM signal has a 4.7K pull up to VIO_1V8.
J2.7	VIO_1V8	(See Schematic)	(See Schematic)	O	1.8V	Voltage reference output created on Torpedo.
J2.8	BT_PCM_DR	C3(PMIC)	GPIO.16/ BT.PCMVDR/ DIG.MIC.CLK0 (PMIC)	I/O	1.8V	TPS65950 GPIO available to user. Connected to TPS65950 GPIO.16.
J2.9	USB1_ID	R11(PMIC)	ID (PMIC)	I/O	5.0V	Tie to pin four of a USB 2.0 OTG compliant connector. This signal negotiates host/device operation with an external USB product. See example Torpedo Launcher design for reference components.
J2.10	BT_PCM_DX	C5 (PMIC)	GPIO.17/ BT.PCM.VDX/ DIG.MIC.CLK1 (PMIC)	I/O	1.8V	TPS65950 GPIO available to user. Connected to TPS65950 GPIO.17.
J2.11	USB1_VBUS	(See Schematic)	(See Schematic)	I/O	5.0V (see note 2)	Ties to pin one of a USB 2.0 OTG compliant connector. This signal indicates to the USB controller that an external USB Host has been connected or can provide power to USB Device peripherals. See example Torpedo Launcher design for reference components.
J2.12	LCD_HSYNC	D26	DSS_HSYNC/GPIO_67	O	1.8V	LCD Horizontal Sync signal.
J2.13	USB1_VBUS	(See Schematic)	(See Schematic)	I/O	5.0V (see note 2)	Ties to pin one of a USB 2.0 OTG compliant connector. This signal indicates to the USB controller that an external USB Host has been connected or can provide power to USB Device peripherals. See example Torpedo Launcher design for reference components.
J2.14	LCD_VSYNC	D27	DSS_VSYNC/GPIO_68	O	1.8V	LCD Vertical Sync Signal.
J2.15	TWL_32K_CLK_OUT	N10(PMIC) AE25	32KCLKOUT (PMIC) SYS_32K	O	1.8V	TPS65950 32kHz clock output.
J2.16	LCD_MDISP	E27	DSS_ACBIAS/GPIO_69	O	1.8V	LCD MDISP signal.
J2.17	T2_REGEN	A10(PMIC)	REGEN (PMIC)	O	Max 4.5V (MAIN_BATTERY)	Active high. External LDO enable signal generated by the TPS65950.

J2 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J2.18	LCD_D6 (G1)	E26	DSS_D6/ UART1_TX/GPIO_76	O	1.8V	LCD G1 data bit when operating in 16 bpp 5:6:5 color mode.
J2.19	5V	(See Schematic)	(See Schematic)	I	4.8V-7V	5V power input. Used by power management controller to charge external MAIN_BATTERY supply.
J2.20	LCD_D20	E28	DSS_D20/SDI_DEN/ McSPI3_SOMI/ DSS_DATA2/GPIO_90	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the *OMAP35x TRM* for LCD bus mapping.
J2.21	5V	(See Schematic)	(See Schematic)	I	4.8V-7V	5V power input. Used by power management controller to charge external MAIN_BATTERY supply.
J2.22	LCD_D9 (G4)	G26	DSS_D9/GPIO_79	O	1.8V	LCD G4 data bit when operating in 16 bpp 5:6:5 color mode.
J2.23	5V	(See Schematic)	(See Schematic)	I	4.8V-7V	5V power input. Used by power management controller to charge external MAIN_BATTERY supply.
J2.24	LCD_D8 (G3)	F27	DSS_D8/GPIO_78	O	1.8V	LCD G3 data bit when operating in 16 bpp 5:6:5 color mode.
J2.25	5V	(See Schematic)	(See Schematic)	I	4.8V-7V	5V power input. Used by power management controller to charge external MAIN_BATTERY supply.
J2.26	LCD_D7 (G2)	F28	DSS_D7/ UART1_RX/GPIO_77	O	1.8V	LCD G2 data bit when operating in 16 bpp 5:6:5 color mode.
J2.27	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J2.28	LCD_DCLK	D28	DSS_PCLK/GPIO_66	O	1.8V	LCD Data Clock output.
J2.29	CSI_D5	A25	CAM_D5/ SSI2_RDY_RX/ GPIO_104	I	1.8V	Camera Sensor Interface Data bit 5.
J2.30	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J2.31	CSI_D2	B24	CAM_D2/ SSI2_RDY_TX/ GPIO_101	I	1.8V	Camera Sensor Interface Data bit 2.
J2.32	SD1_CLK	N28	MMC1_CLK/ MS_CLK/ GPIO_120	O	3.0V (VMMC1)	MMC/SD1 Clock signal.
J2.33	CSI_D3	C24	CAM_D3/ SSI2_DAT_RX/ GPIO_102	I	1.8V	Camera Sensor Interface Data bit 3.
J2.34	LCD_D19	H25	DSS_D19/ SDI_HSYNC/ McSPI3_SIMO/ DSS_DATA1/ GPIO_89	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the *OMAP35x TRM* for LCD bus mapping.

J2 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J2.35	CSI_D4	D24	CAM_D4/ SSI2_FLAG_RX/ GPIO_103	I	1.8V	Camera Sensor Interface Data bit 4.
J2.36	LCD_D18	H26	DSS_D18/ SDI_VSYNC/ McSPI3_CLK/ DSS_DATA0/ GPIO_88	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the *OMAP35x TRM* for LCD bus mapping.
J2.37	uP_UARTB_CTS	H18	UART3_CTS_RCTX/ GPIO_163	I	1.8V	Clear To Send signal for UART3.
J2.38	BATT_LINE	J25	HDQ_SIO/ SYS_ALTCLK/ I2C2_SCCBE/ I2C3_SCCBE/GPIO_170	I/O	1.8V	Bi-directional battery management ONEWIRE interface. This signal has a 4.7K pull-up to VIO_1V8.
J2.39	uP_UARTB_RTS	H19	UART3_RTS_SD/ GPIO_164	O	1.8V	Ready To Send signal for UART3.
J2.40	LCD_D21	J26	DSS_D21/SDI_STP/ McSPI3_CS0/ DSS_DATA3/GPIO_91	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the *OMAP35x TRM* for LCD bus mapping.
J2.41	uP_UARTB_RX	H20	UART3_RX_IRRX/ GPIO_165	I	1.8V	Serial Data Receive signal for UART3.
J2.42	SD1_CMD	M27	MMC1_CMD/MS_BS/ GPIO_121	I/O	3.0V (VMMC1)	MMC/SD1 Command signal. This signal requires a 10K pull-up to VMMC1.
J2.43	uP_UARTB_TX	H21	UART3_TX_IRTX/ GPIO_166	O	1.8V	Serial Data Transmit signal for UART3.
J2.44	SD1_DATA2	N25	MMC1_DAT2/ MS_DAT2/GPIO_124	I/O	3.0V (VMMC1)	MMC/SD1 Data 2 signal. This signal requires a 10K pull-up to VMMC1.
J2.45	MCSPI4_CS0	K26	McBSP1_FSX/ McSPI4_CS0/ McBSP_FSX/GPIO_161	O	1.8V	McSPI4 interface chip select 0 output.
J2.46	SD1_DATA1	N26	MMC1_DAT1/ MS_DAT1/ GPIO_123	I/O	3.0V (VMMC1)	MMC/SD1 Data 1 signal. This signal requires a 10K pull-up to VMMC1.
J2.47	MCBSP2_DX	M21 K4 (PMIC)	McBSP2_DX/GPIO_119 I2S.DIN/TDM.DIN (PMIC)	O	1.8V	McBSP2 interface transmit output.
J2.48	SD1_DATA0	N27	MMC1_DAT0/MS_DAT0/GPIO_122	I/O	3.0V (VMMC1)	MMC/SD1 Data 0 signal. This signal requires a 10K pull-up to VMMC1.
J2.49	MCBSP2_CLKX	L3 (PMIC) N21	I2S.CLK/TDM.CLK (PMIC) McBSP2_CLKX/ GPIO_117	O	1.8V	McBSP2 transmit clock output.
J2.50	SD1_DATA3	P28	MMC1_DAT3/ MS_DAT3/GPIO_125	I/O	3.0V (VMMC1)	MMC/SD1 Data 3 signal. This signal requires a 10K pull-up to VMMC1.

J2 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J2.51	MCBSP2_FSX	K6 (PMIC) P21	I2S.SYNC/TDM.SYNC (PMIC) McBSP2_FSX/ GPIO_116	I/O	1.8V	McBSP2 transmit frame synchronization.
J2.52	SD1_DATA4	P27	MMC1_DAT4/SIM_IO/ GPIO_126	I/O	1.8V	MMC/SD1 Data 4 signal. (see note 3)
J2.53	MCBSP2_DR	K3 (PMIC) R21	I2S.DOUT/ TDM.DOUT (PMIC) McBSP2_DR/GPIO_118	I	1.8V	McBSP2 interface receive input.
J2.54	SD1_DATA5	P26	MMC1_DAT5/SIM_CLK/ GPIO_127	I/O	1.8V	MMC/SD1 Data 5 signal. (see notes 3 and 4)
J2.55	R92 Populated: KEY_ROW3 (CONFIG15)	K7 (PMIC)	KPD.R3 (PMIC)	I/O	1.8V	Keypad Row 3 signal.
	R93 Populated **(default)**: CSI_D7 (CONFIG15)	L28	CAM_D7/GPIO_106	I	1.8V	Camera Sensor Interface Data bit 7.
J2.56	SD1_DATA6	R27	MMC1_DAT6/ SIM_PWRCTRL/ GPIO_128	I/O	1.8V	MMC/SD1 Data 6 signal. (see notes 3 and 4)
J2.57	R92 Populated: KEY_ROW2 (CONFIG14)	L8 (PMIC)	KPD.R2 (PMIC)	I/O	1.8V	Keypad Row 2 signal.
	R93 Populated **(default)**: CSI_D6 (CONFIG14)	K28	CAM_D6/GPIO_105	I	1.8V	Camera Sensor Interface Data bit 6.
J2.58	SD1_DATA7	R25	MMC1_DAT7/SIM_RST/ GPIO_129	I/O	1.8V	MMC/SD1 Data 7 signal. (see note 3)
J2.59	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J2.60	TV_OUT2	W28 W27	TV_OUT2 TV_VFB2	O	1.8V (VDAC)	Analog TV_OUT2.
J2.61	R92 Populated: KEY_ROW1 (CONFIG13)	K8 (PMIC)	KPD.R1 (PMIC)	I/O	1.8V	Keypad Row 1 signal.
	R93 Populated **(default)**: CAM_WEN (CONFIG13)	B23	CAM_WEN/ CAM_SHUTTER/ GPIO_167	I	1.8V	Camera Sensor Write Enable.
J2.62	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J2.63	R92 Populated: KEY_ROW0 (CONFIG12)	K9 (PMIC)	KPD.R0 (PMIC)	I/O	1.8V	Keypad Row 0 signal.
	R93 Populated **(default)**: CSI_HSYNC (CONFIG12)	A24	CAM_HS/ SSI2_DAT_TX/GPIO_94	I/O	1.8V	Camera Sensor Interface Horizontal Sync signal.

J2 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J2.64	TV_OUT1	Y28 Y27	TV_OUT1 TV_VFB1	O	1.8V (VDAC)	Analog TV_OUT1.
J2.65	R94 populated: KEY_COL3 (CONFIG19)	F7 (PMIC)	KPD.C3 (PMIC)	I/O	1.8V	Keypad Column 3 signal.
	R95 Populated **(default)**: CSI_VSYNC (CONFIG19)	A23	CAM_VS/ SSI2_FLAG_TX/ GPIO_95	I/O	1.8V	Camera Sensor Interface Vertical Sync signal.
J2.66	LCD_D14 (R4)	AA28	DSS_D14/SDI_DAT3N/ GPIO_84	O	1.8V	LCD R4 data bit when operating in 16 bpp 5:6:5 color mode.
J2.67	R94 Populated: KEY_COL2 (CONFIG18)	G6 (PMIC)	KPD.C2 (PMIC)	I/O	1.8V	Keypad Column 2 signal.
	R95 Populated **(default)**: CSI_PCLK (CONFIG18)	C27	CAM_PCLK/GPIO_97	I	1.8V	Camera Sensor Interface Pixel Clock signal.
J2.68	LCD_D13 (R3)	AB27	DSS_D13/SDI_DAT2P/ GPIO_83	O	1.8V	LCD R3 data bit when operating in 16 bpp 5:6:5 color mode.
J2.69	R94 Populated: KEY_COL1 (CONFIG17)	H7 (PMIC)	KPD.C1 (PMIC)	I/O	1.8V	Keypad Column 1 signal.
	R95 Populated **(default)**: CSI_XCLKB (CONFIG17)	B26	CAM_XCLKB/GPIO_111	O	1.8V	Camera Sensor Clock Output b.
J2.70	LCD_D12 (R2)	AB28	DSS_D12/ SDI_DAT2N/GPIO_82	O	1.8V	LCD R2 data bit when operating in 16 bpp 5:6:5 color mode.
J2.71	R94 Populated: KEY_COL0 (CONFIG16)	G8 (PMIC)	KPD.C0 (PMIC)	I/O	1.8V	Keypad Column 0 signal.
	R95 Populated **(default)**: CSI_XCLKA (CONFIG16)	C25	CAM_XCLKA/GPIO_96	O	1.8V	Camera Sensor Clock Output a.
J2.72	uP_UARTC_TX	AA25	UART2_TX/ MCBSP3_CLKX/ GPT11_PWM_EVT/ GPIO_146	O	1.8V	Serial Data Transmit signal for UART2.
J2.73	R88 Populated: MCBSP5_DX (CONFIG7)	AF13	ETK_D6/McBSP5_DX/ MMC3_DAT2/ HSUSB1_DATA6/ HSUSB1_TLL_DATA6/ GPIO_20	O	1.8V	McBSP5 interface transmit output.
	R89 Populated **(default)**: MCSPI4_SOMI (CONFIG7)	U21	McBSP1_DR/ McSPI4_SOMI/ McBSP3_DR/GPIO_159	I	1.8V	McSPI4 interface receive input.

J2 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J2.74	uP_UARTC_RTS	AB25	UART2_RTS/ MCBSP3_DR/ GPT10_PWM_EVT/ GPIO_145	O	1.8V	Ready To Send signal for UART2.
J2.75	R88 Populated: MCBSP5_FSX (CONFIG6)	AH9	ETK_D5/McBSP5_FSX / MMC3_DAT1/ HSUSB1_DATA5/ HSUSB1_TLL_DATA5/ GPIO_19	I/O	1.8V	McBSP5 transmit frame synchronization.
	R89 Populated **(default)**: MCSPI4_SIMO (CONFIG6)	V21	McBSP1_DX/ McSPI4_SIMO/ McBSP3_DX/GPIO_158	O	1.8V	McSPI4 interface transmit output.
J2.76	uP_UARTC_CTS	AB26	UART2_CTS/ MCBSP3_DX/ GPT9_PWM_EVT/ GPIO_144	I	1.8V	Clear To Send signal for UART2.
J2.77	R88 Populated: MCBSP5_DR (CONFIG5)	AE11	ETK_D4/McBSP5_DR/ MMC3_DAT0/ HSUSB1_DATA4/ HSUSB1_TLL_DATA4/ GPIO_18	I	1.8V	McBSP5 interface receive input.
	R89 Populated **(default)**: MCSPI4_CLK (CONFIG5)	Y21	McBSP1_CLKR/ McSPI4_CLK/ SIM_CD/GPIO_156	O	1.8V	McSPI4 serial clock signal.
J2.78	LCD_D15 (R5)	AA27	DSS_D15/SDI_DAT3P/ GPIO_85	O	1.8V	LCD R5 data bit when operating in 16 bpp 5:6:5 color mode.
J2.79	LCD_D2 (B3)	AG23	DSS_D2/DX1/GPIO_72	O	1.8V	LCD B3 data bit when operating in 16 bpp 5:6:5 color mode.
J2.80	LCD_D22	AC27	DSS_D22/SDI_CLKP/ GPIO_92	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the *OMAP35x TRM* for LCD bus mapping.
J2.81	LCD_D3 (B4)	AH23	DSS_D3/DY1/GPIO_73	O	1.8V	LCD B4 data bit when operating in 16 bpp 5:6:5 color mode.
J2.82	LCD_D10 (G5)	AD28	DSS_D10/SDI_DAT1N/ GPIO_80	O	1.8V	LCD G5 data bit when operating in 16 bpp 5:6:5 color mode.
J2.83	LCD_D1 (B2)	AH22	DSS_D1/UART1_RTS/ DY0/GPIO_71	O	1.8V	LCD B2 data bit when operating in 16 bpp 5:6:5 color mode.
J2.84	LCD_D11 (R1)	AD27	DSS_D11/SDI_DAT1P/ GPIO_81	O	1.8V	LCD R1 data bit when operating in 16 bpp 5:6:5 color mode.

J2 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J2.85	CSI_D0	AG17	CAM_D0/CSI2_DX2/ GPIO_99	I	1.8V (VAUX4) (see note 5)	Camera Sensor Interface Data bit 0. This signal may also be used as GPI; output signaling is not supported. **NOTE:** The VAUX4 supply is off by default and must be enabled by software.
J2.86	uP_UARTC_RX	AD25	UART2_RX/ MCBSP3_FSX/ GPT8_PWM_EVT/ GPIO_147	I	1.8V	Serial Data Receive signal for UART2.
J2.87	CSI_D1	AH17	CAM_D1/CSI2_DY2/ GPIO_100	I	1.8V (VAUX4) (see note 5)	Camera Sensor Interface Data bit 1. This signal may also be used as GPI; output signaling is not supported. **NOTE:** The VAUX4 supply is off by default and must be enabled by software.
J2.88	uP_CLKOUT1_26MHz	AG25	SYS_CLKOUT1/ GPIO_10	O	1.8V	Processor SYS_CLKOUT1.
J2.89	SYS_BOOT5	AE21	SYS_BOOT5/ MMC2_DIR_DAT3/ GPIO_7	I/O	1.8V	Processor SYS_BOOT5. Must be left floating during boot up, unless the boot order is to be modified. Can be used as GPIO after boot up. This signal has a 4.7K pull-up on the SOM. See Table 5.1 for more information.
J2.90	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J2.91	uP_I2C2_SDA	AE15	I2C2_SDA/ GPIO_183	I/O	1.8V	I2C channel 2 data signal. This signal has a 4.7K pull-up to the reference voltage onboard.
J2.92	MSTR_nRST	A13(PMIC) AH25	NRESPWRON SYS_nRESPWRON	I	1.8V	Active low. External reset input to the Torpedo SOM. This signal should be used to reset all devices on the Torpedo SOM including the CPU.
J2.93	uP_I2C2_SCL	AF15	I2C2_SCL/GPIO_168	I/O	1.8V	I2C channel 2 clock signal. This signal has a 4.7K pull-up to the reference voltage onboard.
J2.94	LCD_D4 (B5)	AG24	DSS_D4/ UART3_RX_IRRX/DX2/ GPIO_74	O	1.8V	LCD B5 data bit when operating in 16 bpp 5:6:5 color mode.
J2.95	uP_I2C3_SCL	AF14	I2C3_SCL/GPIO_184	I/O	1.8V	I2C channel 3 Clock signal. This signal has a 470 ohm pull-up on the SOM.
J2.96	LCD_D5 (G0)	AH24	DSS_D5/ UART3_TX_IRTX/DY2/ GPIO_75	O	1.8V	LCD G0 data bit when operating in 16 bpp 5:6:5 color mode.
J2.97	uP_I2C3_SDA	AG14	I2C3_SDA/GPIO_185	I/O	1.8V	I2C channel 3 Data signal.

J2 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
						This signal has a 470 ohm pull-up on the SOM.
J2.98	LCD_D0 (B1)	AG22	DSS_D0/UART1_CTS/ DX0/GPIO_70	O	1.8V	LCD B1 data bit when operating in 16 bpp 5:6:5 color mode.
J2.99	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J2.100	SYS_BOOT0	AH26	SYS_BOOT0/GPIO_2	I/O	1.8V	Processor SYS_BOOT0. Must be left floating during boot up, unless the boot order is to be modified. Can be used as GPIO after boot up. This signal has a 4.7K pull-up on the SOM. See Table 5.1 for more information.

TABLE NOTES:

1. USB voltage levels follow the *USB 2.0 Specification* and depend on the USB operating speed. Please see the *USB 2.0 Specification* for more information.

2. USB1_VBUS can be used to charge a battery. Please see TI's *TPS65950 OMAP Power Management TRM* and Logic PD's *AN416 OMAP35x Torpedo SOM Power Management* for more information.

3. If used for MMC, this signal requires a 10K pull-up to VIO_1V8. Also, VMMC1 must be set to 1.8V to enable the MMC1 port to operate at 1.8V. If not used for MMC, may be used as a GPIO.

4. This signal is used as card detect on the Zoom OMAP35x Torpedo Development Kit and is recognized as such by Logic PD software. If using the OMAP35x Torpedo SOM on a custom baseboard that uses an SD card socket without card detect, this signal must be grounded.

5. This signal is on the OMAP35x processor's VDDS_CSI2 power rail. On the OMAP35x Torpedo SOM, this rail is powered by the TPS65950's VAUX4 power supply which is not enabled by default; therefore, the signal will not function until this power supply is turned on. Also, this signal is only available as an input when configured as a GPIO.

7.3 Configurable Pins

Several pins are configurable to allow for maximum customization of the OMAP35x Torpedo SOM feature-set. However, tradeoffs must be considered. Table 7.1 gives some examples of features that are gained and lost through customization. Please note that this is not an exhaustive list.

Table 7.1: Feature Gain/Loss through Customization

Resistor Population	Gain	Loss
R92, R94	4x4 Keypad	Camera Interface control signals
R91, R93, R95	12-bit Camera Interface	ADC, 4x4 Keypad

Resistor Population	Gain	Loss
R86	24-bit LCD	SD3, McSPI1 extra CS
R87	SD3, McSPI1 extra CS	24-bit LCD
R88	McBSP5	McSPI4
R89	McSPI4	McBSP5
R90	ADC	Camera interface data8-data11
R97, R86	McSPI3 (with clock)	SD3
R96, R87	SD3	McSPI3

NOTE: Resistor populations other than the default require a custom model number to be created through Logic PD's New Product Introduction (NPI) process. Please contact Logic PD for more information.

Table 7.2 provides a list of all the configurable pins on the J1 and J2 expansion connectors. The information below is the same as what appears in the complete pin description tables in Sections 7.1 and 7.2.

Table 7.2: Configurable J1 and J2 Connector Pins

Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J1.99	LCD_D16	G25	DSS_D16/GPIO_86	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the *OMAP35x TRM* for LCD bus mapping.
	SD3_CMD	AE10	ETK_CTL/ MMC3_CMD/ HSUSB1_CLK/ HSUSB1_TLL_CLK/ GPIO_13	O	1.8V	MMC/SD3 Command signal. This signal requires a 10K pull-up to VIO_1V8.
J1.86	LCD_D17	H27	DSS_D17/GPIO_87	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the *OMAP35x TRM* for LCD bus mapping.
	MCSPI1_CS2	AB1	McSPI1_CS2/ MMC3_CLK/ GPIO_176	O	1.8V	McSPI1 interface chip select 2 output.
J1.78	ADCIN1	J3(PMIC)	ADCIN1 (PMIC)	I	1.5V	Analog to digital converter input. Connected to TPS65950 ADCIN1.
	CSI_D9	L27	CAM_D9/GPIO_108	I	1.8V	Camera Sensor Interface Data bit 9.
J1.76	ADCIN0	H4 (PMIC)	ADCIN0 (PMIC)	I	1.5V	Analog to digital converter input. Connected to TPS65950 ADCIN0.
	CSI_D8	K27	CAM_D8/GPIO_107	I	1.8V	Camera Sensor Interface Data bit 8.
J2.63	KEY_ROW0	K9 (PMIC)	KPD.R0 (PMIC)	I/O	1.8V	Keypad Row 0 signal.
	CSI_HSYNC	A24	CAM_HS/ SSI2_DAT_TX/GPIO_94	I	1.8V	Camera Sensor Interface Horizontal Sync signal.

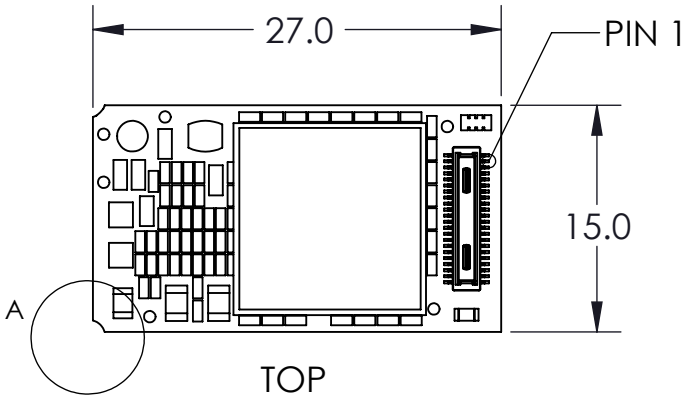
Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J2.61	KEY_ROW1	K8 (PMIC)	KPD.R1 (PMIC)	I/O	1.8V	Keypad Row 1 signal.
	CAM_WEN	B23	CAM_WEN/ CAM_SHUTTER/ GPIO_167	I	1.8V	Camera Sensor Write Enable.
J2.57	KEY_ROW2	L8 (PMIC)	KPD.R2 (PMIC)	I/O	1.8V	Keypad Row 2 signal.
	CSI_D6	K28	CAM_D6/GPIO_105	I	1.8V	Camera Sensor Interface Data bit 6.
J2.55	KEY_ROW3	K7 (PMIC)	KPD.R3 (PMIC)	I/O	1.8V	Keypad Row 3 signal.
	CSI_D7	L28	CAM_D7/GPIO_106	I	1.8V	Camera Sensor Interface Data bit 7.
J2.71	KEY_COL0	G8 (PMIC)	KPD.C0 (PMIC)	I/O	1.8V	Keypad Column 0 signal.
	CSI_XCLKA	C25	CAM_XCLKA/GPIO_96	O	1.8V	Camera Sensor Clock Output a.
J2.69	KEY_COL1	H7 (PMIC)	KPD.C1 (PMIC)	I/O	1.8V	Keypad Column 1 signal.
	CSI_XCLKB	B26	CAM_XCLKB/GPIO_111	O	1.8V	Camera Sensor Clock Output b.
J2.67	CSI_PCLK	G6 (PMIC)	KPD.C2 (PMIC)	I	1.8V	Camera Sensor Interface Pixel Clock signal.
	KEY_COL2	C27	CAM_PCLK/GPIO_97	I/O	1.8V	Keypad Column 2 signal.
J2.65	KEY_COL3	F7 (PMIC)	KPD.C3 (PMIC)	I/O	1.8V	Keypad Column 3 signal.
	CSI_VSYNC	A23	CAM_VS/ SSI2_FLAG_TX/ GPIO_95	I	1.8V	Camera Sensor Interface Vertical Sync signal.
J1.87	LCD_D23	AC28	DSS_D23/ SDI_CLKN/ GPIO_93	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the *OMAP35x TRM* for LCD bus mapping.
	SD3_CLK	AF10	ETK_CLK/ McBSP5_CLKX/ MMC3_CLK/ HSUSB1_STP/ MM1_RXDP/ HSUSB1_TLL_STP/ GPIO_12	O	1.8V	MMC/SD3 Clock signal. This signal requires a 10K pull-up to VIO_1V8.
J1.96	SD3_DATA0	AE4	MMC2_DAT4/ MMC2_DIR_DAT0/ MMC3_DAT0/GPIO_136	I/O	1.8V	MMC/SD3 Data 0 signal. This signal requires a 10K pull-up to VIO_1V8.
	MCSPI3_CS1	AH14	ETK_D7/ McSPI3_CS1/ MMC3_DAT7/ HSUSB1_DATA3/ MM1_TXEN_n/ HSUSB1_TLL_DATA3/ GPIO_21	O	1.8V	McSPI3 interface chip select 1 output.

Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J1.94	SD3_DATA1	AH3	MMC2_DAT5/ MMC2_DIR_DAT1/ CAM_GLOBAL_RESET / MMC3_DAT1/ HSUSB3_TLL_STP/ MM3_RXDP/GPIO_137	I/O	1.8V	MMC/SD3 Data 1 signal. This signal requires a 10K pull-up to VIO_1V8.
	MCSPI3_CS0	AH12	ETK_D2/McSPI3_CS0 / HSUSB1_DATA2/ MM1_TXDAT/ HSUSB1_TLL_DATA2/ GPIO_16	O	1.8V	McSPI3 interface chip select 0 output.
J1.92	SD3_DATA2	AF3	MMC2_DAT6/ MMC2_DIR_CMD/ CAM_SHUTTER/ MMC3_DAT2/ HSUSB3_TLL_DIR/ GPIO_138	I/O	1.8V	MMC/SD3 Data 2 signal. This signal requires a 10K pull-up to VIO_1V8.
	MCSPI3_SIMO	AF11	ETK_D0/ McSPI3_SIMO/ MMC3_DAT4/ HSUSB1_DATA0/ MM1_RXRCV/ HSUSB1_TLL_DATA0/ GPIO_14	O	1.8V	McSPI3 interface transmit output.
J1.90	SD3_DATA3	AE3	MMC2_DAT7/ MMC2_CLKIN/ MMC3_DAT3/ HSUSB3_TLL_NXT/ MM3_RXDM/ GPIO_139	I/O	1.8V	MMC/SD3 Data 3 signal. This signal requires a 10K pull-up to VIO_1V8.
	MCSPI3_SOMI	AG12	ETK_D1/ McSPI3_SOMI/ HSUSB1_DATA1/ MM1_TXSE0/ HSUSB1_TLL_DATA1/ GPIO_15	I	1.8V	McSPI3 interface receive input.
J1.88	MCSPI3_CLK	AE13	ETK_D3/McSPI3_CLK / MMC3_DAT3/ HSUSB1_DATA7/ HSUSB1_TLL_DATA7/ GPIO_17	O	1.8V	McSPI3 serial clock signal.
	MCSPI1_CS3	AB2	McSPI1_CS3/ HSUSB2_TLL_DATA2/ MM2_TXDAT/ GPIO_177	O	1.8V	McSPI1 interface chip select 3 output.
J2.77	MCBSP5_DR	AE11	ETK_D4/McBSP5_DR/ MMC3_DAT0/ HSUSB1_DATA4/ HSUSB1_TLL_DATA4/ GPIO_18	I	1.8V	McBSP5 interface receive input.
	MCSPI4_CLK	Y21	McBSP1_CLKR/ McSPI4_CLK/ SIM_CD/GPIO_156	O	1.8V	McSPI4 serial clock signal.

Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J2.75	MCBSP5_FSX	AH9	ETK_D5/McBSP5_FSX/ MMC3_DAT1/ HSUSB1_DATA5/ HSUSB1_TLL_DATA5/ GPIO_19	I/O	1.8V	McBSP5 transmit frame synchronization.
	MCSPI4_SIMO	V21	McBSP1_DX/ McSPI4_SIMO/ McBSP3_DX/GPIO_158	O	1.8V	McSPI4 interface transmit output.
J2.73	MCBSP5_DX	AF13	ETK_D6/McBSP5_DX/ MMC3_DAT2/ HSUSB1_DATA6/ HSUSB1_TLL_DATA6/ GPIO_20	O	1.8V	McBSP5 interface transmit output.
	MCSPI4_SOMI	U21	McBSP1_DR/ McSPI4_SOMI/ McBSP3_DR/GPIO_159	I	1.8V	McSPI4 interface receive input.
J1.82	ADCIN3	P11(PMIC)	ADCIN3 (PMIC)	I	max 2.5V	Analog to digital converter input. Connected to TPS65950 ADCIN3.
	CSI_D11	C26	CAM_D11/GPIO_110	I	1.8V	Camera Sensor Interface Data bit 11.
J1.80	ADCIN2	G3 (PMIC)	ADCIN2 (PMIC)	I	max 2.5V	Analog to digital converter input. Connected to TPS65950 ADCIN2.
	CSI_D10	B25	CAM_D10/ SSI2_WAKE/GPIO_109	I	1.8V	Camera Sensor Interface Data bit 10.

Appendix A: Torpedo SOM Mechanical Drawing

REVISIONS			
REV.	PCB NUMBER	DESCRIPTION	DATE
D	1013993, 1017857	UPDATED FOR AM3703 & DM3730 MODELS, ADDED ETM DIMENSIONS	06.21.11
E	1013993, 1017857	ADDED ADDITIONAL PIN NUMBERS TO FOOTPRINT	05.23.12



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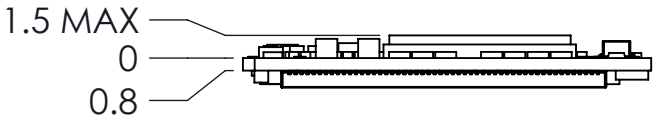

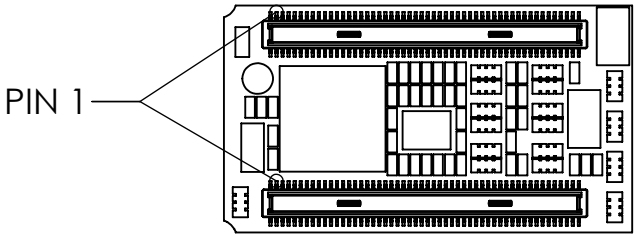

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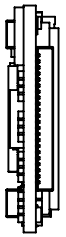
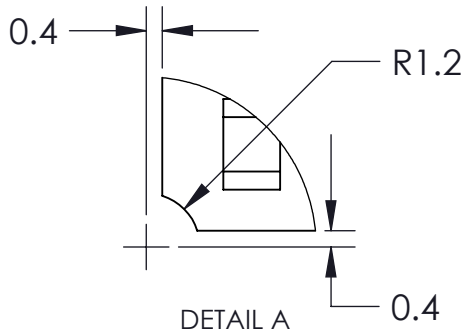


NOTES:

1. DO NOT SCALE DRAWING
2. DO NOT PLACE ANY COMPONENTS WITHIN LAYOUT AREA OF SOM
3. BASEBOARD CONNECTOR SPECIFICATION (MACHINE PLACEMENT RECOMMENDED): HIROSE DF40C-100DS-0.4V
4. IF USING THE ETM DEBUG BOARD DURING DEVELOPMENT, VERIFY COMPONENT HEIGHT CONSTRAINTS IN SPECIFIED AREA
5. PANEL VESTIGES ON ALL FOUR EDGES. PLEASE DO NOT PLACE COMPONENTS DIRECTLY ALIGNED WITH EDGE OF SOM



DETAIL A
SCALE 6 : 1

THIS DRAWING PREPARED IN ACCORDANCE WITH ASME Y14.5-2000

ALL DIMENSIONS ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED

TOLERANCES UNLESS OTHERWISE SPECIFIED

X	± 0.5
X.X	± 0.2
X.XX	± 0.1
X°	± 1°

THIRD ANGLE PROJECTION

ENG	KAG
DATE	06.21.11
CHECK	NWR
DATE	06.21.11
MGR	
DATE	
MANF	
DATE	

LOGIC PD™
411 WASHINGTON AVE. SUITE 400 MINNEAPOLIS, MN 55401
T : 612.672.9495 F : 612.672.9489 I : WWW.LOGICPD.COM

SIZE	TITLE	REV
A	AM3703, DM3730 & OMAP35X TORPEDO SOM	E
SCALE	DWG NO	SHEET
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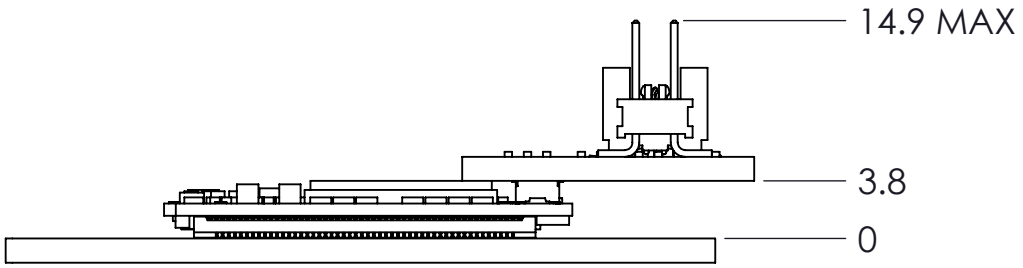
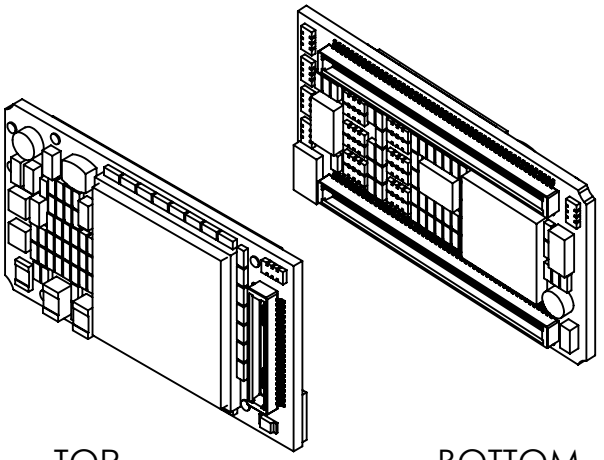
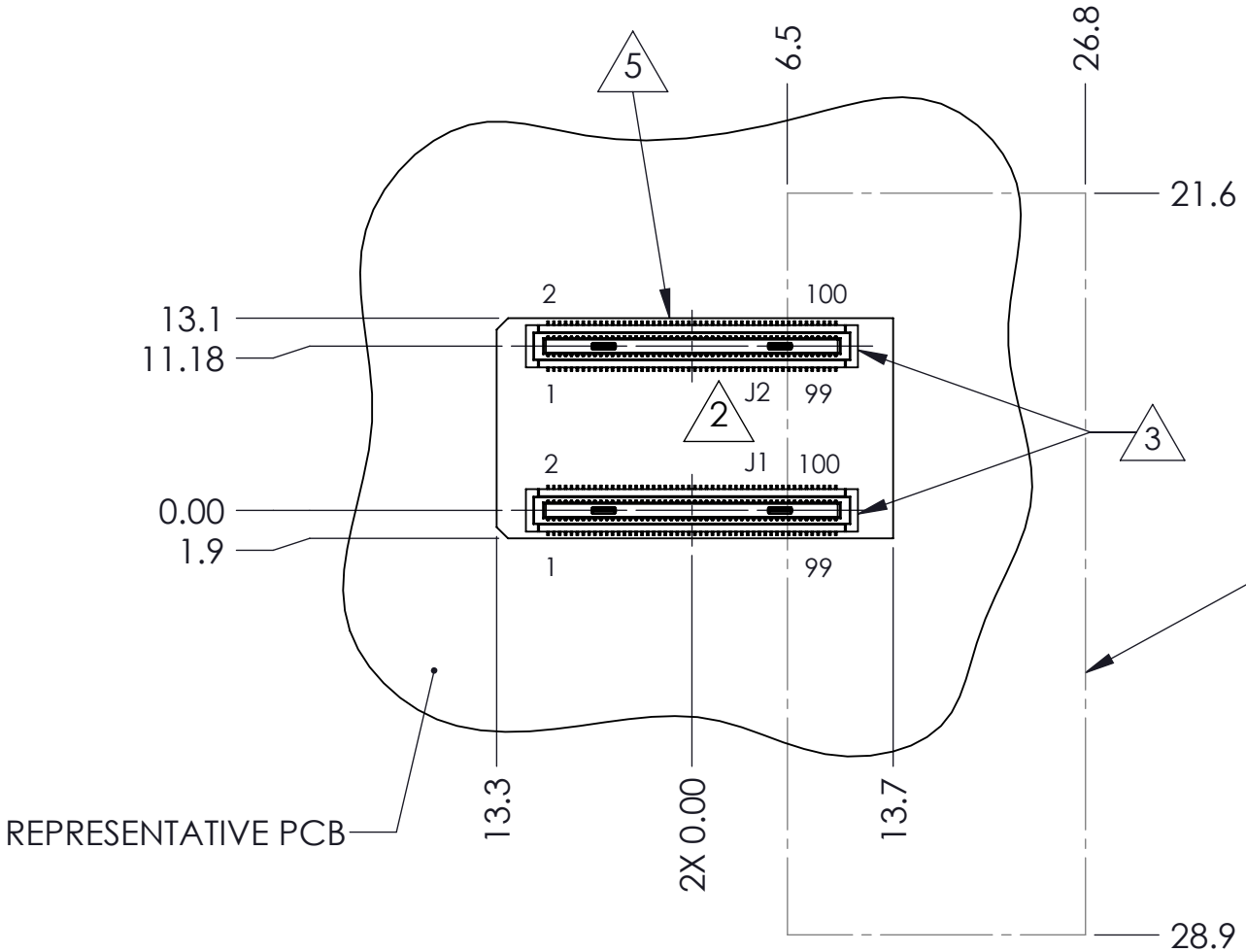


ETM DEBUG BOARD HEIGHT CONSTRAINTS



ISOMETRIC VIEWS
FOR REFERENCE ONLY



RECOMMENDED KEEPOUT AREA AND BASEBOARD FOOTPRINT

SIZE	TITLE	REV
A	AM3703, DM3730 & OMAP35X TORPEDO SOM	E
SCALE	DWG NO	SHEET
2:1	1012857	2 OF 2