Beacon RZ/G2M Development Kit

User Guide

Beacon EmbeddedWorks
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Revision History

REV	EDITOR	DESCRIPTION	SCHEMATIC PN & REV	APPROVAL	DATE
A	A.Ford, E. Fritz B. Brown	Production Release	SOM Schematic 1031615 REV A Baseboard Schematic 1031644 Rev A	AF, EF, BB	Nov. 16, 2023

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1 Introduction

This user guide continues where the QuickStart Guide ended by providing additional hardware details about the Beacon RZ/G2 Development Kit. The purpose of this document is to present information that may be useful after you have unpacked the kit, run through the demo, and are ready to begin development work. This document also references other resources depending upon specific development needs.

1.1 Scope of Document

This user guide does not provide detailed instructions for the software included with the kit. Please refer to the specific user guides for each respective software product for additional information. A list of additional documentation is available in Appendix A: Additional Documentation.

1.2 Requirements

It is assumed that the QuickStart Guide has been read in its entirety. See Appendix A: Additional Documentation for a link to the QuickStart Guide.

The following items will be needed for the procedures described in this document:

- Beacon RZ/G2 Development Kit registered on Beacon EmbeddedWorks' website[1]
- Host PC (the procedures in this document were evaluated using a Windows 10 host PC)
- USB port
- microSD card reader
- microSD card
- Serial cable (USB Type-A standard male to USB Type-B micro male - included in development kit)
- Wattson cable (USB Type-A standard male to USB Type-B mini male - included in development kit)
- Active Internet connection
- Ethernet Cable
- Terminal emulation program (e.g., Tera Term as described in Section 2.2)

[1] http://support.beaconembedded.com/auth/register_product.php

1.3 RZ/G2 Baseboard Features Diagram

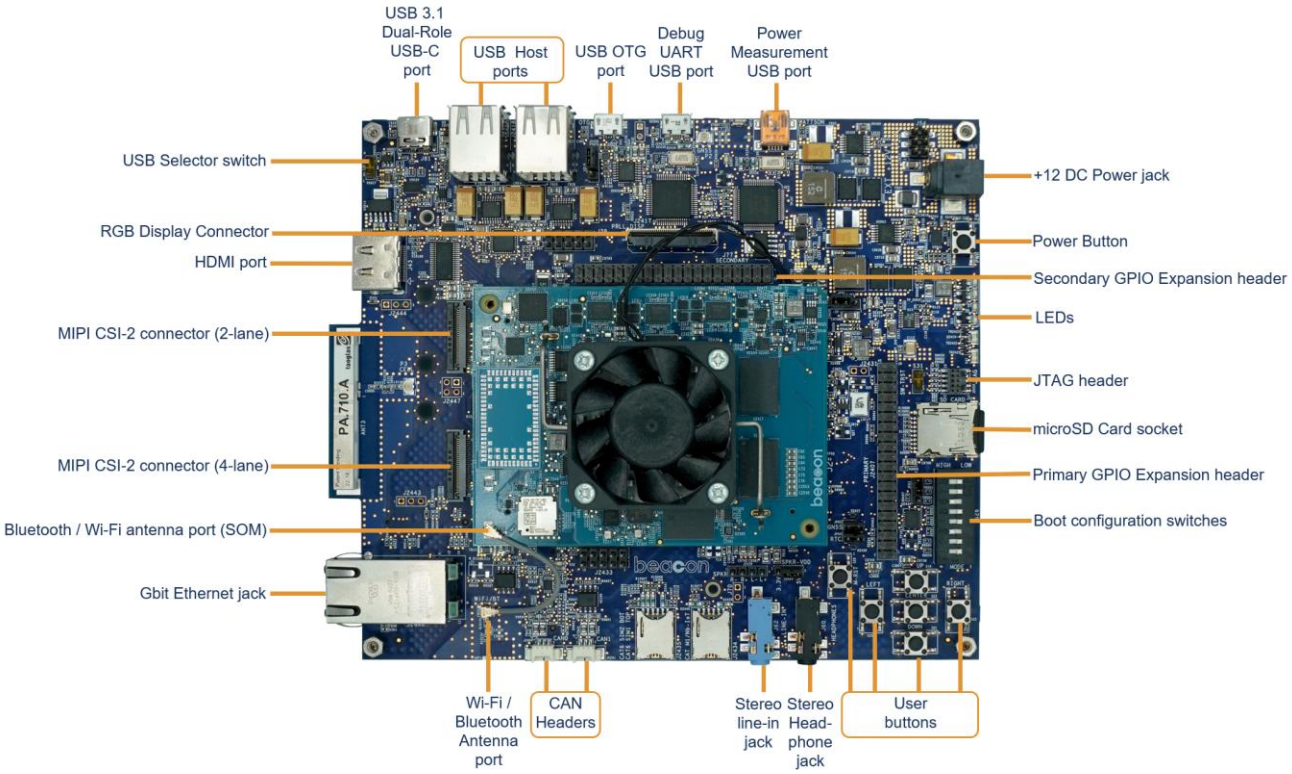

Figure 1: Baseboard (Front Side)

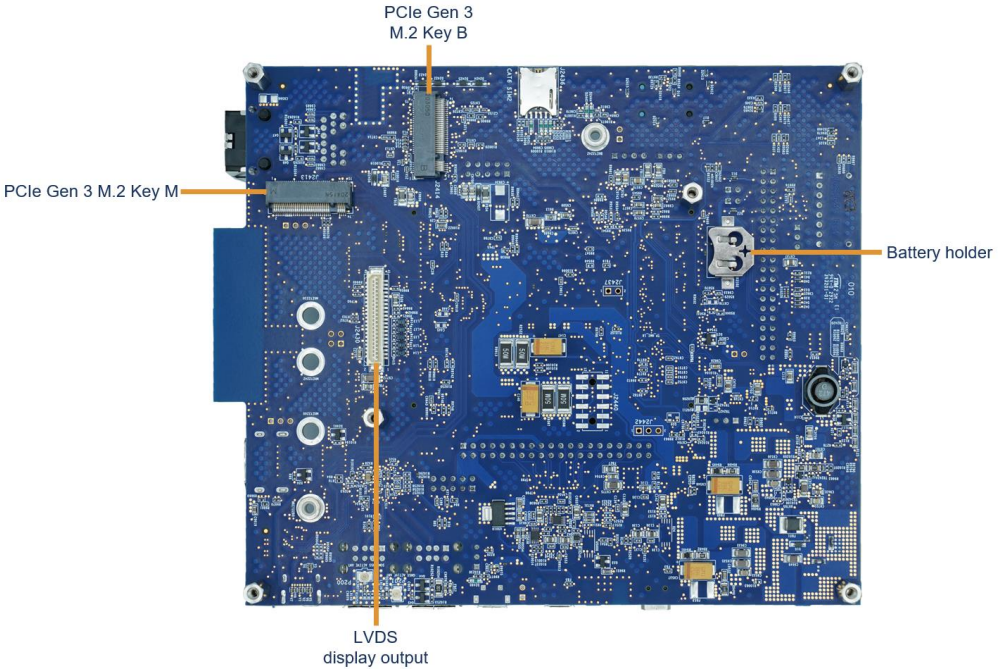

Figure 2: Baseboard (Back Side)

2 Connect Development Kit to PC

To begin development work, the development kit needs to be connected to a host PC. Connect the USB micro-B cable included in the development kit to the serial debug port.

2.1 Connect Using USB Micro-B Cable

Follow the steps below to connect USB micro-B serial debug cable.

1. Connect the USB micro-B cable to the debug UART USB port (J2425) on the baseboard and to an empty USB port on the host PC.

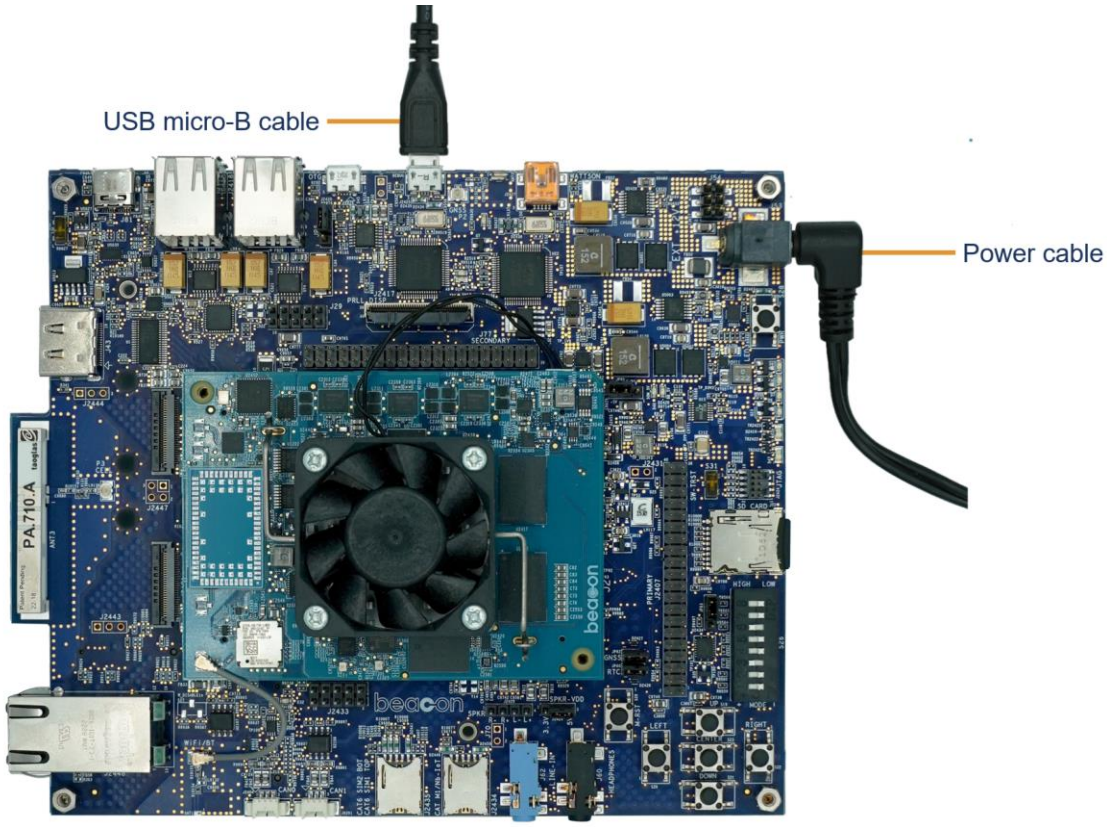

Figure 3: Baseboard (Front Side) w/ Cables

NOTE: The baseboard is equipped with an FTDI virtual COM port (VCP) chip that causes the USB device to appear to the host computer as an additional COM port. Settings for the terminal emulation program will remain the same. However, a driver must be installed on the host computer for proper operation. A link to the driver and instructions for using the USB-to-UART VCP chip can be found in Beacon EmbeddedWorks' USB-to-UART VCP Chip Driver ReadMe[2]. See section 7.10.2 for more information on how to configure the debug terminal.

2. Plug the power supply into an electrical outlet and the power cable output connector into the power-in connector on the baseboard as seen in Figure 3.

[2] http://support.beaconembedded.com/downloads/910/

3. Before powering on the kit, install a terminal emulation program to communicate with the development kit. Proceed to the next section for details.

2.2 Install Terminal Emulator Program

The Beacon RZ/G2 Development Kit is designed to communicate with terminal emulation programs using the included microUSB cable. Although Beacon EmbeddedWorks does not support any particular terminal emulation program, Tera Term for Windows and Minicom for Linux are recommended.

2.2.1 Setup Windows Serial Terminal

Tera Term can be downloaded for free from Beacon EmbeddedWorks' website. To install Tera Term:

1. Download the ZIP file[3] from Beacon EmbeddedWorks' website and extract the contents.
2. After extracting the contents, locate the teraterm-x.xx.exe file and double-click it.
3. Follow the on-screen instructions to install Tera Term.
   a. Baud rate: **115200**
   b. Data: **8 bits**
   c. Parity: **None**
   d. Stop: **1 bit**
   e. Flow control: **None**

NOTE: The communication port assigned to the DUT is usually the first port associated with the USB cable.

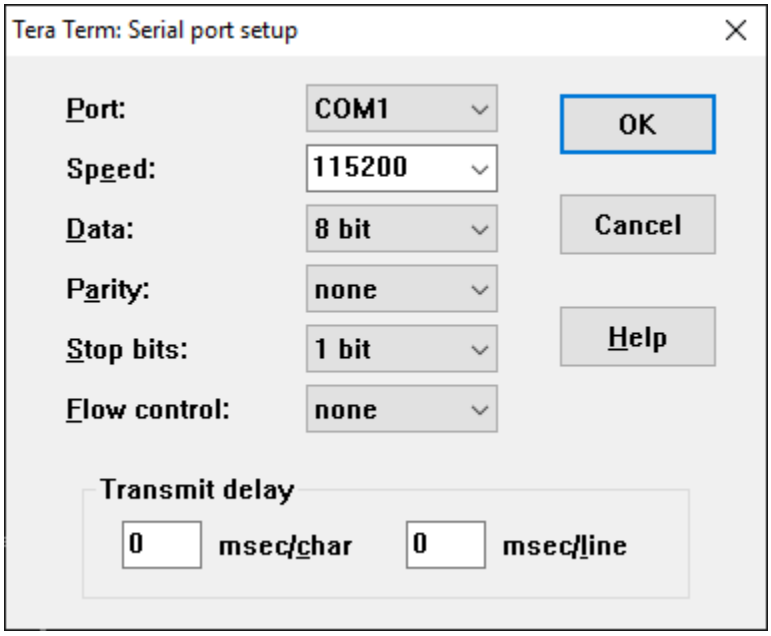

Figure 4: Tera Term Serial Port Settings

[3] http://support.beaconembedded.com/downloads/240/

4. Click ‘OK’
5. Tera Term serial terminal has been completed

2.2.2 Setup Linux Serial Terminal

Follow the directions below for installing Minicom within Ubuntu.

1. To install minicom, run ‘sudo apt install minicom’
2. To setup minicom, type ‘sudo minicom -s’
3. Select ‘Serial port setup’

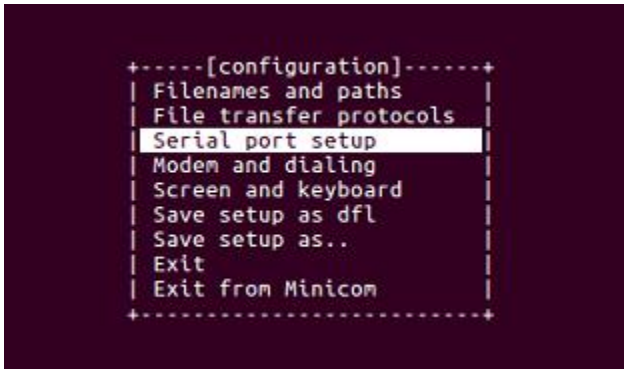

Figure 5: Minicom Configuration Menu

4. Setup the serial port interface specific to the Linux Host PC. This example uses ‘/dev/ttyUSB0’ and the baud rate of 115200 8N1.

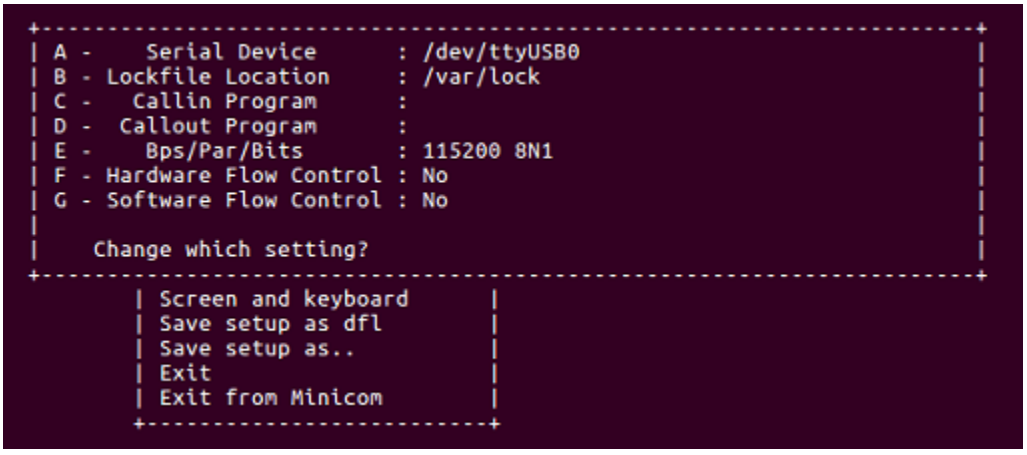

Figure 6: Minicom Serial Port Setup

5. Save setup

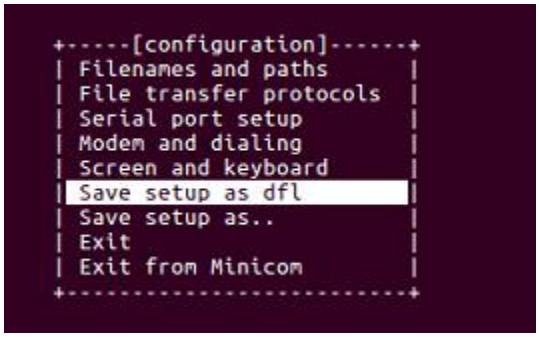

Figure 7: Minicom Save Setup as Default Option

6. Select Exit
7. Minicom serial terminal setup has been completed

2.3 Boot into U-Boot

U-Boot is a bootloader configured by Beacon EmbeddedWorks to provide the capability for loading the operating system (OS) and applications. In addition, it provides a full suite of commands for interfacing to the System on Module (SOM). These commands load the OS, configure hardware platforms, bring up hardware, customize applications, perform tests, and manage in-field devices.

1. Make sure the development kit is set up as described in Section 2.1.
2. Insert the pre-built OS image SD card into the baseboard.
3. Verify the boot switches (S26 on the baseboard) are configured to boot from on-board eMMC. See section 8.1 for boot options. This step is important because U-Boot boots from onboard flash memory even if the Linux will be run the microSD card.

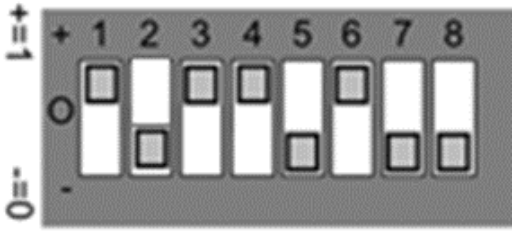

Figure 8: eMMC Switch Settings on S26

4. Start the terminal emulation program on the host PC.
5. Verify that the serial port settings are correct (see section 2.2 in the previous section).
6. Press the power button (S28)
7. In the host PC's terminal emulation program, you should see a U-Boot screen like the one below (version numbers and other details may differ from what is shown).

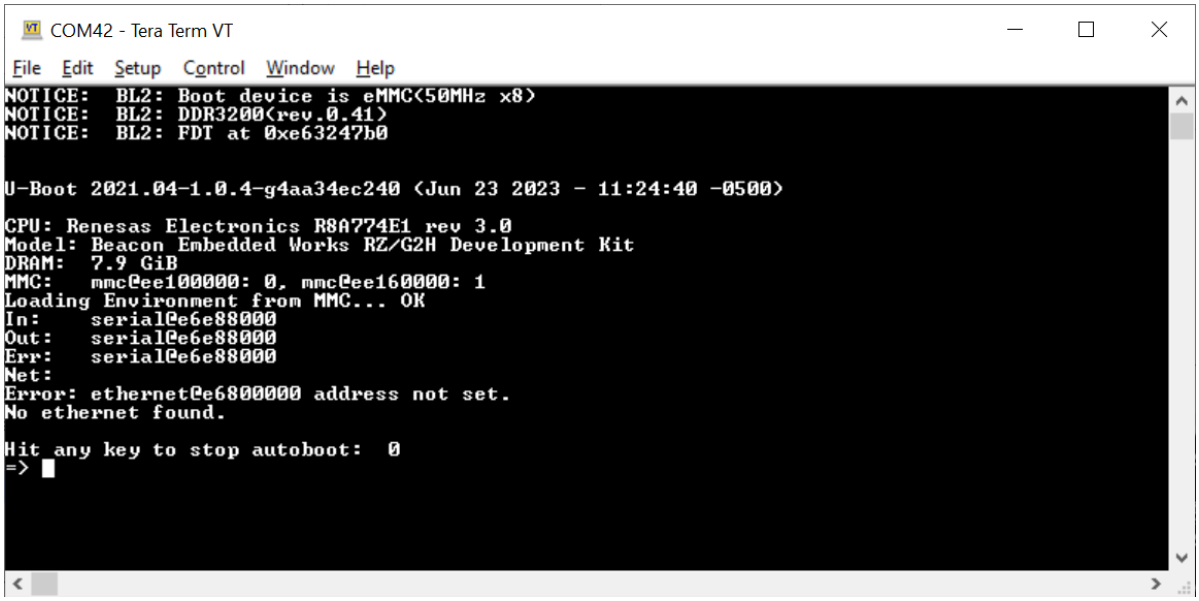

Figure 9: U-Boot Prompt

8. The system is now ready to work with the RZ/G2 SOM using U-Boot. For more information on U-Boot's and its capabilities, please see the RZ/G2 SOM Series Linux User Guide provided by Beacon EmbeddedWorks. This document is available on Beacon EmbeddedWorks' website and the download location is referenced in Appendix A of this document.

3 Wattson

Wattson is a power measurement and performance monitoring application now standard on all Beacon EmbeddedWorks Development Kits.

The application delivers real-time graphical feedback and data-logging capabilities without the need for external oscilloscopes and meters. Wattson guides you to the lowest power and highest performance software combination for the product.

Wattson is instrumental in helping you minimize power in run, idle, standby, suspend, and system-off states, maximizing battery life in the end application. Wattson is independent of the system, allowing power measurement even when the SOM is in deep-sleep states like suspend and even off.

Wattson runs on Windows and Linux PCs, enabling software development on Linux, Android and Windows IOT-based products.

3.1 How to Get Wattson

Follow the steps below to download and install Wattson.

1. Wattson is available for download from Beacon EmbeddedWorks' website. The links below will launch the download for the specific OS running on the host.
   - Wattson for Windows Installer[4] (ZIP file)
   - Wattson for Linux Installer[5] (tar.gz file)

2. Extract the ZIP or tar.gz file. In Linux, the following command will extract the tar.gz:

```
$ tar -xvf wattson_linux.tar.gz
```

In that folder, locate the *HOW TO INSTALL* document containing installation instructions.

3. Once Wattson is installed on the host PC, a Wattson User Guide is available from the Start > Beacon EmbeddedWorks > Wattson User Guide menu or within the Wattson application under the *Help* menu.

[4] https://support.beaconembedded.com/DesktopModules/Bring2mind/DMX/Download.aspx?portalid=0&EntryId=1416
[5] https://support.beaconembedded.com/DesktopModules/Bring2mind/DMX/Download.aspx?portalid=0&EntryId=1418

3.2 Connect the Development Kit for Wattson

For Wattson to interact with the Beacon RZ/G2 Development Kit, use the included USB A to USB mini-B cable to connect the power measurement USB port on the baseboard to an available USB port on the host PC.

It is recommended to first launch Wattson and connect the USB mini-B cable to J2427 before connecting the debug UART cable. This will prevent any issues where Wattson might detect the wrong serial debug interface.

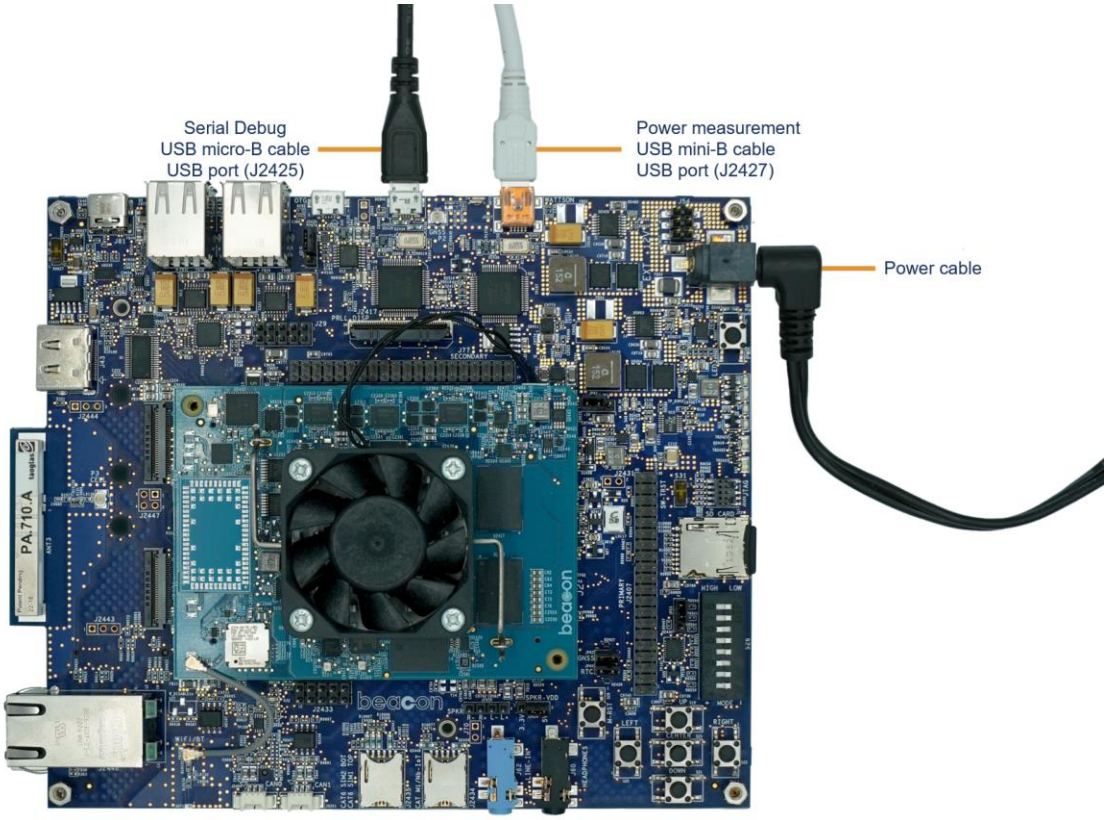

Figure 10: Connect USB mini-B Cable for Wattson

4 Baseboard Jumper Descriptions

The baseboard jumpers are set by default as described in Table 1 and shown in Figure 11.

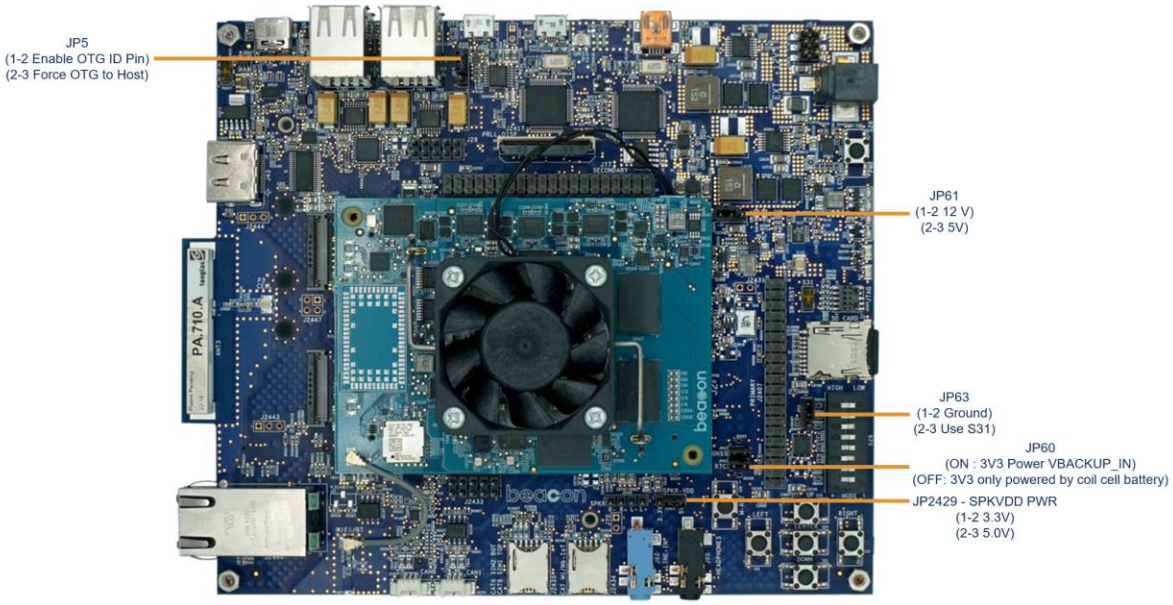

Figure 11: Jumper Locations

Reference Designator	Default Jumper Pin Location	Description
JP5	1-2	Used to allow the OTG pin to use the ID pin from the cable, or force OTG to host-only mode by grounding ID pin.
JP60	1-2	Used to connect the X2102 coin cell battery to the RTC
JP61	2-3	Connect FAN_SUPPLY to 5V.
JP63	2-4	Jumper header can route JTAG nRST to a SPST switch or pull nRST to ground via 1k resistor
JP2429	1-2	Jumper header made available for the audio CODEC for applications where additional power is required to power the SPKVDD supply. Move across pins 2-3 to increase voltage to 5V.

Table 1: Available Jumpers

5 Connect Antenna to the RZ/G2 SOM

The RZ/G2 SOM provides a U.FL connector receptacle at location P1 for connecting a 50-ohm dual-band antenna for WiFi and Bluetooth wireless connectivity. The kit will come with a Johanson Technology 2450AD14A5500T antenna attached to the Wi-Fi/Bluetooth module. This antenna is located on the baseboard.

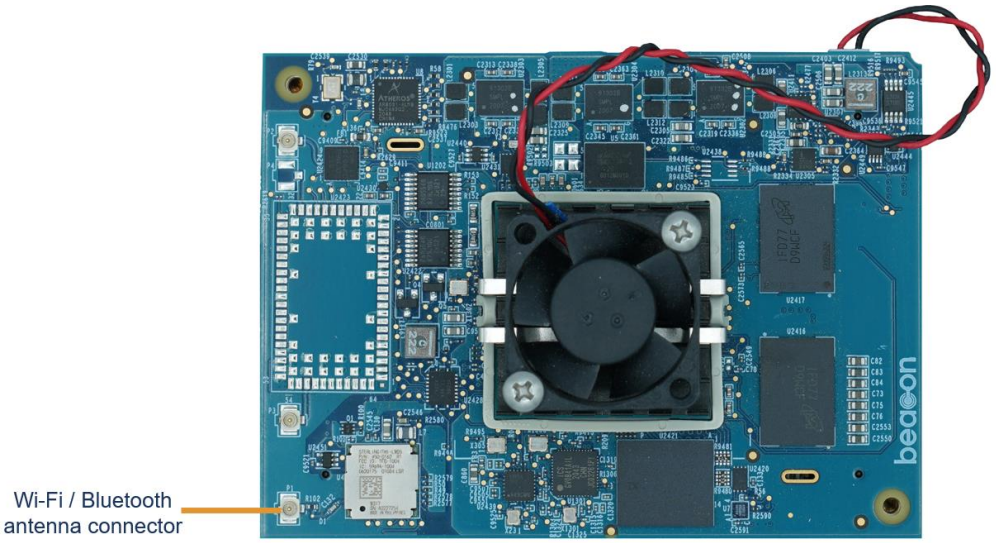

Figure 12: RZ/G2 SOM (Front Side)

IMPORTANT NOTE: The antenna connector on the SOM is very fragile. Take extreme care when connecting and disconnecting the antenna. If antenna movement is likely in an end-product design, Beacon EmbeddedWorks suggests designing supports or reinforcements for the antenna and cable on the baseboard in order to prevent damage to the connector.

There are two additional antenna options that are certified for Laird Sterling-LWB5 wireless module used on the RZ/G2 SOM. Each is connected to the SOM with a thin cable and U.FL connector.

5.1 Flex Planar Inverted F Antenna (FlexPIFA)

One antenna option is the Laird 001-0016 Flexible Planar Inverted F Antenna (FlexPIFA). The FlexPIFA option is a 3-dBi 50-ohm PCB trace antenna attached to 100 mm miniature coaxial cable with a U.FL connector at the far end. The FlexPIFA supports dual bands: 2.4 GHz and 5.5 GHz.

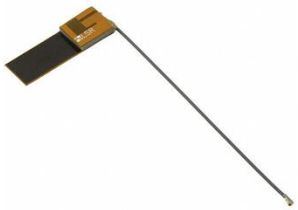

Figure 13: Laird 2.4GHZ/5.5GHZ PCB Trace Antenna and Integrated Cable

1. When using this option, connect the U.FL connector at the end of the FlexPIFA to the U.FL connector receptacle at location P1 on the SOM.
2. The back of the FlexPIFA surface has adhesive to help secure the antenna at the desired location.

5.2 2.4/5.5 GHz Dipole Antenna

The second option is the LSR 001-0009 2.4/5.5 GHz Dipole Antenna. This 50-ohm dipole antenna has +2dBi peak gain at both 2.4 GHz and 5 GHz. This whip tilt antenna is integrated with a with reverse polarity SMA connector.

To connect to the SOM, this option will also require the LSR 080-0001 Cable Assembly. This cable adaptor assembly is 105mm in length with reverse polarity SMA Female bulkhead connector on one end and a U.FL connector on the other end using 1.13mm diameter coaxial cable.

Figure 14: LSR 2.4GHZ/5.5GHZ Dipole Antenna and Adaptor Cable

1. When using this option, connect the SMA connector of cable adaptor assembly to the dipole antenna.
2. Next connect the U.FL connector of cable adaptor assembly to the U.FL connector receptacle at location P1 on the SOM.

6 Powering Down the Development Kit

To provide a graceful shutdown, it is recommended that users use a combination of software and hardware to power down the development kit.

First the user must submit the poweroff command. Using the poweroff command allows the system to terminate running processes, save any unsaved data, close open files, and perform other shutdown-related tasks in an orderly manner. This helps prevent data corruption, file system damage, and other issues that may occur when abruptly cutting power to a running system.

```
root# poweroff
```

The user may also press and hold S28 (ON/OFF) to force the system to power down. This will work in the event of a system lock-up or process that is stuck in a loop. Using S28 to power down in this manner will not allow the system to terminate running processes, save data, close files or perform other shutdown-related tasks in an orderly manner.

Afterwards to power the system back on, press the switch S28 (ON/OFF) button on the baseboard.

7 Functional Specifications

The block diagram for the Beacon RZ/G2 Development Kit is shown below.

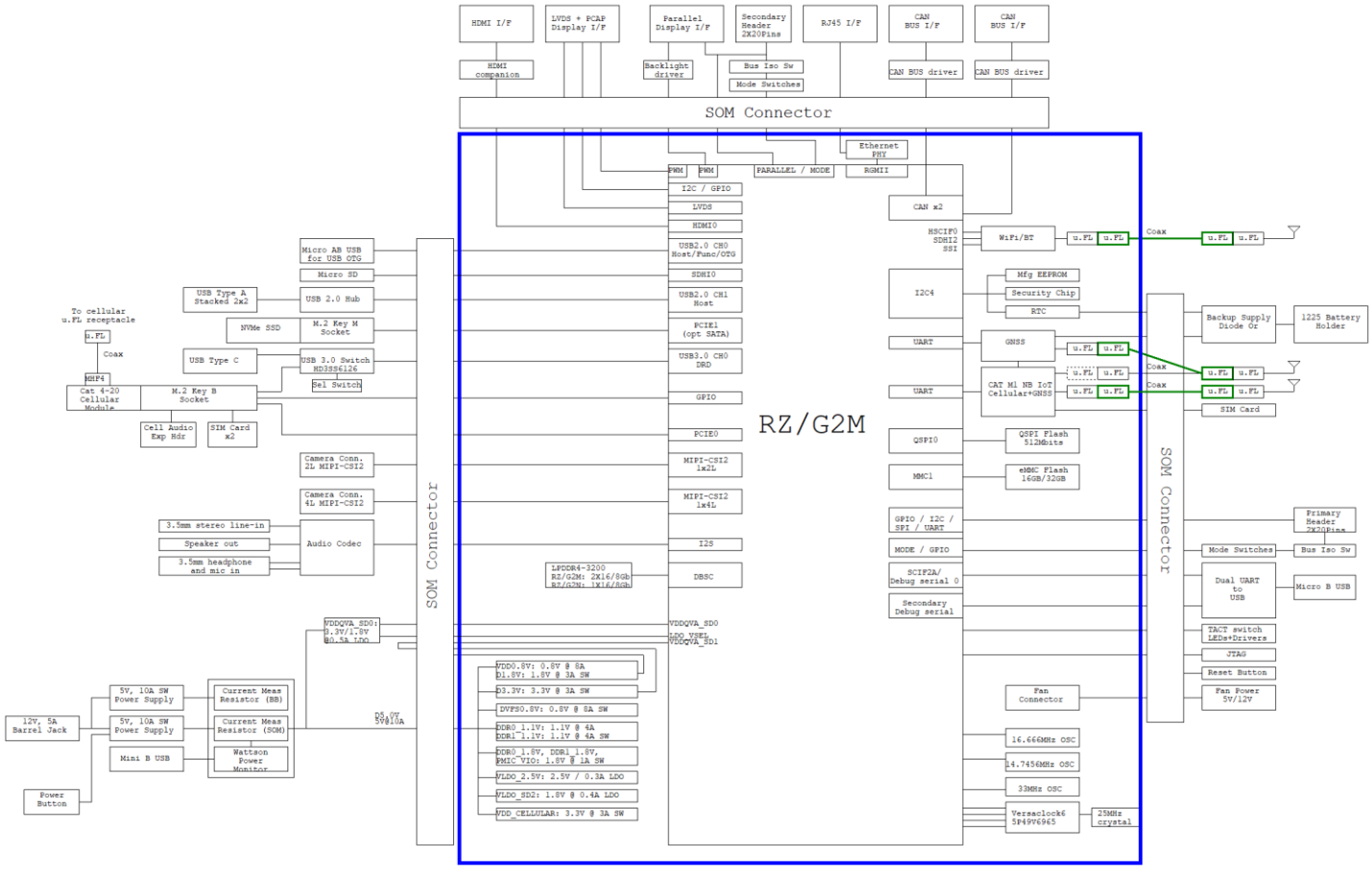

Figure 15: RZ/G2 Dev Kit Block Diagram

7.1 SOM to Baseboard Interface

The baseboard includes two Samtec BSH-090-01-L-D-A-TR, 180-pin, double row, 0.5 mm pitch SMT receptacle connectors at locations J1 and J2 for hosting the SOM. All power, grounds, and digital signals traverse through these three host connectors.

For the detailed pin mapping of the SOM to baseboard connectors, please refer to section 11.

7.2 Clocks

Information in this section describes the various clocks used on the RZ/G2 development kit.

7.2.1 SOM Clocks

Clocks seen on the SOM are used for the processor, display, Ethernet and USB.

7.2.1.1 Processor Clocks

The RZ/G2 processor requires two reference clocks: one for system and high-speed functions and another for low-frequency functions. The high-speed clock connects directly to the processor and the low-speed clock is connected indirectly through the RTC.

Parameter	Min	Typical	Max	Unit
High-speed Processor Crystal (X305)	--	16.6666	--	MHz
Low-speed Crystal (via RTC – Y3)	--	32.768	--	kHz

Table 2: Processor Clocks

7.2.1.2 Other On-board Clocks

There is also a programmable clock generator on the SOM to provide clock references for Display Dot clocks, the Ethernet controller, and the USB as enumerated below and referenced as U2439. The programmable clock generator is controlled via software, and the clocks are enabled and disabled on demand. The clock frequencies are specified in the device tree.

Parameter	Min	Typical	Max	Unit
Display Dot Clock0 (LVDS Clock via U2439)	--	33	--	MHz
Display Dot Clock1 (X1302)	--	33	--	MHz
Display Dot Clock2/3 (RBG Clock via U2439)	--	33	--	MHz
USB XTAL (via U2429)	--	50	--	MHz
Ethernet Ref Clock (via U2429)	--	125	--	MHz
Ethernet PHY Ref Clock (Y4)	--	25.000	--	MHz
Clock Generator Ref Clock (X23)	--	25.000	--	MHz
SCIF Ref Clock (X1303)	--	14.7456	--	MHz
PCIe Clock Generator (U1301)	--	100.000	--	MHz
PCIe Clock Generator Ref Clock (X1301)	--	25.000	--	MHz

Table 3: Other On-board SOM Clocks

7.2.2 Baseboard Clocks

The baseboard also includes clocks for various functions as listed below.

Parameter	Min	Typical	Max	Unit
USB Hub Oscillator (Y10)	--	24.000	--	MHz
Wattson FTDI USB to UART Crystal (Y2)	--	12.000	--	MHz
Debug FTDI USB to UART Crystal (Y13)	--	12.000	--	MHz
Audio Clock-A (via U2429)	--	24.576	--	MHz
Audio Clock-B (via U2429)	--	22.5792	--	MHz
Audio Clock-Codec (via U2429)	--	24.000	--	MHz

Table 4: Baseboard Clocks

7.3 Embedded Memory

There are memories available on the SOM and the baseboard of the RZ/G2 development kit.

7.3.1 SOM Memory

The SOM has LPDDR4, eMMC, QSPI NOR flash and a serial EEPROM. See the RZ/G2 Hardware specification for more details on these memories.

7.3.2 Baseboard Memory

The baseboard provides a microSD Card socket at location J72 (see Figure 1: Baseboard (Front Side) for a picture which includes the microSD card socket).

The processor for RZ/G2 SOM supports up to three SD Host Interface (SDHI) capable of the standard SDIO and SDXC protocol. The SOM reserves SDHI0 for use on the baseboard using a 4-bit data interface for SD Cards.

In addition, the RZ/G2 processors allow designers to select the voltage levels at which the SDHI0 interface operates. The SDHI specification requires +3.3V operation by default and can later negotiate +1.8V signaling if supported by the target. The RZ/G2 SOM wires in GPIO6_30 signal to allow the system to switch the interface voltage.

SDHI2 operates at 400 kHz (low-speed), 25MHz (normal-speed mode), 50MHz (high-speed mode) or 200MHz (ultra high-speed). The SDHI2 can operate at either +3.3V or +1.8V depending on the operating mode.

7.4 Display Interfaces

The RZ/G2 SOM provides an HDMI interface, a two 4-lane LVDS interface, and a 24-bit RGB interface which are routed directly out to the SOM interface connectors. The RGB interface pins are multiplexed with other devices, so enabling it may require disabling other uses for the corresponding pins.

7.4.1 HDMI

The baseboard brings the SOM HDMI signals to a 19-pin HDMI receptacle connector that carries the HDMI display interface, I2C control lines, power, and ground to an external HDMI display.

The HDMI receptacle (Samtec HDMI-19-01-F-SM) is located at J43. See Figure 1: Baseboard (Front Side) which includes the HDMI port at the left of the picture. This 19-pin HDMI high-speed receptacle meets digital display working group single monitor interface specifications.

The pin mapping for the 19-pin HDMI receptacle is shown in the table below. The receptacle also includes four through-hole ground tails for grounding the connector shell.

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain
1	HDMI0_TMDSDATAP2	HDMI Data 2+	O	5.0V	5V_HDMI_IN
2	DGND	Digital Ground	PWR	GND	--
3	HDMI0_TMDSDATAN2	HDMI Data 2-	O	5.0V	5V_HDMI_IN
4	HDMI0_TMDSDATAP1	HDMI Data 1+	O	5.0V	5V_HDMI_IN
5	DGND	Digital Ground	PWR	GND	--
6	HDMI0_TMDSDATAN1	HDMI Data 1-	O	5.0V	5V_HDMI_IN
7	HDMI0_TMDSDATAP0	HDMI Data 0+	O	5.0V	5V_HDMI_IN
8	DGND	Digital Ground	PWR	GND	--
9	HDMI0_TMDSDATAN0	HDMI Data 0-	O	5.0V	5V_HDMI_IN
10	HDMI0_TMDSCLKP	HDMI Clock+	O	5.0V	5V_HDMI_IN
11	DGND	Digital Ground	PWR	GND	--
12	HDMI0_TMDSCLKN	HDMI Clock-	O	5.0V	5V_HDMI_IN
13	HDMI0_CEC	HDMI Consumer Electronics Control	I/O	5.0V	5V_HDMI_IN
14	NC	No Connect	--	--	--
15	HDMI0_SCL	DDC_CLK_OUT	O	5.0V	5V_HDMI_IN
16	HDMI0_SDA	DDC_DAT_OUT	I/O	5.0V	5V_HDMI_IN
17	DGND	Digital Ground	PWR	GND	--
18	5V_HDMI_OUT	+5V Power	PWR	5.0V	5V_HDMI_IN
19	HDMI_HPD	EARC N/HOTPLUG_DET_OUT	I	5.0V	5V_HDMI_IN

Table 5: HDMI Receptacle (J43) Pin Mappings

7.4.2 LVDS

The LVDS signals are each connected to a 41-pin display header connector that carries the LVDS display interface, capacitive touch I2C, control lines, power and backlight PWM control to an external display board.

The LVDS display header connector (Hirose DF9-41P-1V(32)) is located at J2430 on the back of the baseboard. See Figure 2 for a picture which includes the LVDS display output in the center left area. This 41-pin board-to-board header complies with the standard connector specification for the flat panel display interfaces, VESA FPDI-1 Standard Interface Connector.

The pin mapping for the 41-pin LVDS display header connector is shown in the table below.

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain
1	DISP_3V3	3.3V Logic power supply	PWR	3.3V	DISP_3V3_IN
2	DISP_3V3	3.3V Logic power supply	PWR	3.3V	DISP_3V3_IN
3	DGND	Ground	PWR	GND	--
4	DGND	Ground	PWR	GND	--
5	T_LVDS0_CH0_P	LVDS differential pair	O	3.3V	VDDQ18_LVDS
6	T_LVDS0_CH0_N	LVDS differential pair	O	3.3V	VDDQ18_LVDS
7	DGND	Ground	PWR	GND	--
8	T_LVDS0_CH1_P	LVDS differential pair	O	3.3V	VDDQ18_LVDS
9	T_LVDS0_CH1_N	LVDS differential pair	O	3.3V	VDDQ18_LVDS
10	DGND	Ground	PWR	GND	--
11	T_LVDS0_CH2_P	LVDS differential pair	O	3.3V	VDDQ18_LVDS
12	T_LVDS0_CH2_N	LVDS differential pair	O	3.3V	VDDQ18_LVDS
13	DGND	Ground	PWR	GND	--
14	T_LVDS0_CH3_P	LVDS differential pair	O	3.3V	VDDQ18_LVDS
15	T_LVDS0_CH3_N	LVDS differential pair	O	3.3V	VDDQ18_LVDS
16	DGND	Ground	PWR	GND	--
17	T_LVDS0_CLK_P	LVDS differential clock	O	3.3V	VDDQ18_LVDS
18	T_LVDS0_CLK_N	LVDS differential clock	O	3.3V	VDDQ18_LVDS
19	DGND	Ground	PWR	GND	--
20	R_LCD_PWM2	GPIO assigned for PWM to backlight (PWM2_A/GPIO2_08)	O	3.3V	D3.3V
21	R_LCD_RESET	GPIO assigned for LCD reset (GP5_3)	O	3.3V	D3.3V
22	R_LCD_PWR	GPIO assigned for enabling LCD power (I/O Expander 1.IO1)	O	3.3V	DISP_3V3
23	GP5_9_TOUCH_INTn	GPIO assigned for interrupt from touch (GP5_9)	I	3.3V	DISP_3V3
24	DGND	Ground	PWR	GND	--
25	I2C5_SCL	I2C clock signal to cap touch	O	3.3V	D3.3V
26	I2C5_SDA	I2C data signal to/from cap touch	I/O	3.3V	D3.3V
27	DGND	Ground	PWR	GND	--
28	Reserved	Reserved for test point	--	--	--
29	DGND	Ground	PWR	GND	--
30	BB_5V	5V Backlight power supply	PWR	5.0V	BB_5V_IN
31	BB_5V	5V Backlight power supply	PWR	5.0V	BB_5V_IN
32	BB_5V	5V Backlight power supply	PWR	5.0V	BB_5V_IN
33	BB_5V	5V Backlight power supply	PWR	5.0V	BB_5V_IN
34	R_LCD_SELECT	Level-shifted GPIO assigned LCD select (GPIO_EXP_3V3_P1_2)	O	3.3V	DISP_3V3
35	LCD_BACKLIGHT_EN	Level-shifted GPIO assigned backlight enable (GPIO_EXP_3V3_P1_3)	O	3.3V	DISP_3V3
36	LCD_TOUCH_SHDWN	Level-shifted GPIO assigned touch shutdown (GPIO_EXP_3V3_P1_4)	O	3.3V	DISP_3V3
37	LCD_H_POL	Level-shifted GPIO assigned horizontal polarity (GPIO_EXP_3V3_P1_5)	O	3.3V	DISP_3V3
38	LCD_V_POL	Level-shifted GPIO assigned vertical polarity ((GPIO_EXP_3V3_P1_6)	O	3.3V	DISP_3V3
39	GND	Ground	PWR	GND	--
40	GND	Ground	PWR	GND	--
41	GND	Ground	PWR	GND	--

Table 6: LVDS Connector (J2430) Pin Mapping Network

7.5 Connectivity

The RZ/G2 development kit offers Wi-Fi, Bluetooth, and Gig Ethernet.

7.5.1 Wi-Fi and Bluetooth

The Beacon RZ/G2 Development Kit has incorporated the Sterling-LWB5 wireless module by Laird to provide WiFi and Bluetooth wireless connectivity. The LWB5 module provides 2.4GHz and 5GHz 802.11a/b/g/ac Wi-Fi along with Bluetooth v4.2 + Bluetooth Low-Energy (BLE) functionality based on the Cypress CYW43353 chipset. The wireless module is located on the SOM and includes a U.FL connector for attaching an antenna. See section 5 for instructions on connecting the antenna.

7.5.2 Wired Ethernet 10/100/1000 MAC + PHY

The Beacon RZ/G2 Development Kit supports 10/100/1000 Mbps Ethernet.

The RZ/G2 processor includes an internal Ethernet Media Access Controller (MAC) designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. The RZ/G2 SOM design completes the interface to one media with a Microchip KSZ9131 10/100/1000 PHY attached to the RGMII interface of the processor.

The baseboard provides an Ethernet RJ-45 jack (J2448) with integrated magnetics. See Figure 1: Baseboard (Front Side) for a picture which includes the Ethernet 10/100/1000 jack at the left bottom.

7.6 Security Features

The RZ/G2 SOM includes NXP's A7102CHUK/T0BC2VAZ Plug & Trust secure element for end-to-end security.

The A71CH is a ready-to-use solution providing a root of trust at the IC level and proven, chip-to-cloud security right out of the box. It is a platform capable of securely storing and provisioning credentials, securely connecting IoT devices to cloud services and performing cryptographic node authentication.

It can be used with various host platforms and host operating systems to secure a broad range of applications.

7.7 USB Interfaces

The Beacon RZ/G2 Development Kit supports USB 3.1 Gen 1 Dual Role port.

The RZ/G2 processor supports two dual-role interfaces (USB1 and USB2). The USB interfaces are routed directly from the processor to the SOM Host connector.

7.7.1 USB Dual Role Port

The baseboard routes the USB1 interface from the SOM to a USB-C connector on the baseboard (J81). See Figure 1: Baseboard (Front Side) for a picture which includes the USB-C dual-role port connector at the top left edge of the baseboard.

This USB-C port is capable of sourcing up to 3.0A @ 5V but may be limited by the amount of power pulled from the power supply.

7.7.2 USB OTG Port

The baseboard routes the USB OTG interface from the SOM to a micro-USB connector on the baseboard (J2420). See Figure 1: Baseboard (Front Side) for a picture which includes the USB-OTG port connector at the top edge near the center.

This USB OTG port is capable of sourcing up to 0.6A, but it is limited by the amount of power pulled in from the power supply.

7.7.3 USB Host Ports

The baseboard routes the USB2 interface from the SOM to a 4-port USB hub component consisting of four USB 4 host ports. The four USB Type A receptacle connectors are two dual-stacked USB connectors locations J2418, and J2419.

See Figure 1: Baseboard (Front Side) for a picture which includes the two dual-USB Host port connectors along the top left edge of the baseboard.

The USB Host ports are mapped as follows:

- USB Host 1 – J2419 - top (500mA)
- USB Host 2 – J2419 - bottom (500mA)
- USB Host 3 – J2418 - top (500mA)
- USB Host 4 – J2418 - bottom (500mA)

7.8 Audio

7.8.1 Serial Sound Interface (SSI)

The Beacon RZ/G2 Development Kit implements three of the SOM's serial sound interfaces (SSI) modules.

- SSI0 and SS11_A provide playback to the WM8962 CODEC.
- SSI2 provides playback to the HDMI which is done internally within the processor.

7.8.2 Audio CODEC

The baseboard provides an Audio CODEC with 24-bit resolution from Cirrus Logic Inc., part number WM8962BECSN/R. The Audio CODEC can drive stereo headphones, drive at least one low-power speaker, and sample data from stereo line input. The Audio CODEC includes an Inter-IC Sound (I2S) interface for connection to the SOM using the SSI0 and SS1 interfaces.

To allow full software control over all its features, the Audio CODEC supports a 2-wire (I2C) serial control interface mode, with full read-back capability on all registers. The baseboard uses the SOM's I2C5 bus for this interface.

Refer to Figure 1: Baseboard (Front Side) for a picture identifying the various audio connections discussed below.

7.8.2.1 Audio In/Out – Stereo Headphones

The baseboard provides a black 3.5mm audio jack at location J60 for stereo headphones. The pin mapping for the 6-pin 3.5mm stereo headphones audio jack is shown in the table below.

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain	Notes
1	HP_POLE2	Microphone In	I	3.3V	3V3_AUD	--
2	HP_L	Headphone Left Channel	O	3.3V	1V8_AUD	--
3	HP_R	Headphone Right Channel	O	3.3V	1V8_AUD	--
4	HP_POLE1	Analog Ground	PWR	GND	--	--
5	RFU	--	--	--	--	--
6	HP_DET	Headphone Detect (M_MD1 GP0_2_HP_DET)	I	3.3V	3V3_AUD	1

Table 7: 6-pin 3.5mm Stereo Headphones Jack (J60) Pin Mapping

The black 3.5mm audio jack is configured by default using the pin assignment as defined by the American Headset Jack (AHJ) standard. The baseboard can be configured to use the open mobile terminal platform (OMTP) standard by removing R696 and R698 and then populating both R697 and R662. See how the signals are assigned to the various connections of the 4-pole male end in the figure below.

Figure 16: CTIA versus OMTP

7.8.2.2 Audio Out – Stereo Line-Out

A stereo audio line-out connection is available on the baseboard at location J26. Stereo line out voltage reference default is 3.3 volts. However, there is an option of applying an external supply (5.0V) if more power is desired for stereo-line out audio.

Stereo audio line-out reference voltage selection is controlled via JP2429. See Figure 11: Jumper Locations.

The pin mapping for the 4-pin stereo line-out header is shown in the table below.

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain
1	SPKRN	Speaker-out Right Channel-Negative	O	3.3/5.0V	SPKVDD
2	SPKRP	Speaker-out Right Channel-Positive	O	3.3/5.0V	SPKVDD
3	SPKLN	Speaker-out Left Channel-Negative	O	3.3/5.0V	SPKVDD
4	SPKLP	Speaker-out Left Channel-Positive	O	3.3/5.0V	SPKVDD

Table 8: 2-pin Stereo Line-Out (J2428) Pin Mappings

7.8.2.3 Audio In – Stereo Line-In

A stereo audio line-in connection is available on the baseboard. The stereo line-in input is available on the baseboard with a blue 3.5mm audio jack at location J62.

The pin mapping for the 6-pin 3.5mm stereo headphones audio jack is shown in the table below.

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain	Notes
1	AGND	Analog Ground	PWR	GND	--	--
2	IN4L_IN	Left channel single-ended input 4	I	1.8V	1V8_AUD	--
3	IN4R_IN	Right channel single-ended input 4	I	1.8V	1V8_AUD	--
4	LINE_IN_DET	Microphone nDetect (M_MD4_GP0_6_LINE_IN_DET)	I	3.3V	D3.3V_SOM	--
5	RFU	--	--	--	--	--
6	RFU	--	--	--	--	--

Table 9: 6-pin 3.5mm Microphone Jack (J62) Pin Mappings

7.9 Camera Interface

The Beacon RZ/G2 Development Kit supports two MIPI CSI-2 interfaces. One interface is 4-lane, and one interface is 2-lane. The MIPI CSI-2 interfaces are routed directly from the processor to the SOM Host connector (see Section 11 Baseboard Connectors - Pin Descriptions & Functions).

The baseboard routes the 4-Lane MIPI CSI-2 interfaces from the SOM Host connector to a MIPI CSI-2 connector J2421 on the baseboard and the 2-Lane MIPI CSI-2 interfaces from the SOM Host connector to a MIPI CSI-2 connector J2438 for external camera connection. See Figure 1: Baseboard (Front Side) for a picture which includes the MIPI CSI-2 connectors flagged on the left side. The connectors support control signals delivered through an I2C bus (I2C2 & I2C5). When connecting to the MIPI CSI-2 interface, it must use a mating connector to the Hirose FH52-28S-0.5SH. The pin mapping for the MIPI CSI-2 connector on the baseboard is shown in the table below.

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain	Notes
1	DGND	Digital Ground	PWR	GND	--	--
2	CSI0_DATAP3	Differential MIPI-CSI2 data signal	I	1.8V	VDDQ18_CSI0	--
3	CSI0_DATAN3	Differential MIPI-CSI2 data signal	I	1.8V	VDDQ18_CSI0	--
4	DGND	Digital Ground	PWR	GND		--
5	CSI0_DATAP2	Differential MIPI-CSI2 data signal	I	1.8V	VDDQ18_CSI0	--
6	CSI0_DATAN2	Differential MIPI-CSI2 data signal	I	1.8V	VDDQ18_CSI0	--
7	DGND	Digital Ground	PWR	GND	--	--
8	CSI0_CLKP	Differential MIPI-CSI2 clock signal	O	1.8V	VDDQ18_CSI0	--
9	CSI0_CLKN	Differential MIPI-CSI2 clock signal	O	1.8V	VDDQ18_CSI0	--
10	DGND	Digital Ground	PWR	GND	--	--
11	CSI0_DATAP1	Differential MIPI-CSI2 data signal	I	1.8V	VDDQ18_CSI0	--
12	CSI0_DATAN1	Differential MIPI-CSI2 data signal	I	1.8V	VDDQ18_CSI0	--
13	DGND	Digital Ground	PWR	GND	--	--
14	CSI0_DATAP0	Differential MIPI-CSI2 data signal	I	1.8V	VDDQ18_CSI0	--
15	CSI0_DATAN0	Differential MIPI-CSI2 clock signal	I	1.8V	VDDQ18_CSI0	--
16	DGND	Digital Ground	PWR	GND	--	--
17	CSI0_RSTN	CSI_nRST - CSI reset signal	I	1.8V	BBD1V8	--
18	SYNC_IN0	RFU	--	--	--	--
19	DGND	Digital Ground	PWR	GND		--
20	CSI0_CAM_SCL	I2C clock for MIPI-CSI2 camera	I/O	1.8V	BBD1V8	--
21	CSI0_CAM_SDA	I2C data for MIPI-CSI2 camera	I/O	1.8V	BBD1V8	--
22	DGND	Digital Ground	PWR	GND	--	--
23	FLASH0	RFU	--	--	--	--
24	SYNC_OUT0	RFU	--	--	--	--
25	BB_5V	Power	PWR	5V0	BB_5V_IN	--
26	BB_5V	Power	PWR	5V0	BB_5V_IN	--
27	BB_5V	Power	PWR	5V0	BB_5V_IN	--
28	DGND	--	PWR	GND	--	--

Table 10: 4-Lane MIPI CSI-2 Connector (J2421) Pin Mappings

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain	Notes
1	DGND	Digital Ground	PWR	GND	GND	--
2	--	--	--	--	--	--
3	--	--	--	--	--	--
4	DGND	Digital Ground	PWR	GND	GND	--
5	--	--	--	--	--	--
6	--	--	--	--	--	--
7	DGND	Digital Ground	PWR	GND	GND	--
8	CSI1_CLKP	Differential MIPI-CSI2 clock signal	O	1.8V	VDDQ18_CSI1	--
9	CSI1_CLKN	Differential MIPI-CSI2 clock signal	O	GND	VDDQ18_CSI1	--
10	DGND	Digital Ground	PWR	GND	--	--
11	CSI1_DATAP1	Differential MIPI-CSI2 data signal	I	1.8V	VDDQ18_CSI1	--
12	CSI1_DATAN1	Differential MIPI-CSI2 data signal	I	1.8V	VDDQ18_CSI1	--
13	DGND	Digital Ground	PWR	GND	GND	--
14	CSI1_DATAP0	Differential MIPI-CSI2 data signal	I	1.8V	VDDQ18_CSI1	--
15	CSI1_DATAN0	Differential MIPI-CSI2 clock signal	I	1.8V	VDDQ18_CSI1	--
16	DGND	Digital Ground	PWR	GND	GND	--
17	CSI1_RSTN	CSI_nRST - CSI reset signal	I	1.8V	BBD1V8	--
18	SYNC_IN1	RFU	--	--	--	--
19	DGND	Digital Ground	PWR	GND	--	--
20	CSI1_CAM_SCL	I2C clock for MIPI-CSI2 camera	I/O	1.8V	BBD1V8	--
21	CSI1_CAM_SDA	I2C data for MIPI-CSI2 camera	I/O	1.8V	BBD1V8	--
22	DGND	Digital Ground	PWR	GND	GND	--
23	FLASH1	RFU	--	--	--	--
24	SYNC_OUT1	RFU	--	--	--	--
25	BB_5V	Power	PWR	5V0	BB_5V_IN	--
26	BB_5V	Power	PWR	5V0	BB_5V_IN	--
27	BB_5V	Power	PWR	5V0	BB_5V_IN	--
28	DGND	Digital Ground	PWR	GND	GND	--

Table 11: 2-Lane MIPI CSI-2 Connector (J2438) Pin Mappings

7.10 UARTS

The Beacon RZ/G2 Development Kit has four UART interfaces driven from the processor.

- SCIF0 (four-wire)
- SCIF2 (two-wire) – primary use is A53 debug
- HSCIF2 (two-wire) - primary use is for a secondary serial console

7.10.1 SCIF0 – GPIO Primary Connector

SCIF0 has TX and RX available with off-board connector options for application use on J2407, the 40-Pin GPIO Primary Connector. SCIF0.RTS0# is not available as the alternate function is being used as I2C2_SCL and SCIF0.CTS0# is also not available as the alternate function for this pin is assigned to GP5_03 and being used as R_LCD_RESET. Please note that by default SCIF0.TX and SCIF0 are configured in the device tree to be available.

7.10.2 SCIF2 and HSCIF2 – Debug Serial Interface

The RZ/G2 SOM dedicates SCIF2 to be used for serial communications on the Cortex-A57 processor and HSCIF2 for a secondary serial console or application purposes.

Both SCIF2 and HSCIF2 are connected to a USB to Dual Port UART Converter (FTDI FT2232D) on the baseboard. The baseboard routes the USB interface from the FTDI converter chip to a USB 2.0 Micro B receptacle connector (J2425) on the baseboard for external serial connection to a PC. See Figure 1: Baseboard (Front Side) for a picture which includes the Debug UART USB Port flagged on the center of the top side. Typically, the Cortex-A57 appears as the lower serial port on the host PC running the terminal emulator. This serial port is used for accessing the Linux debug terminal.

7.11 SPI

The Beacon RZ/G2 Development Kit has routed two MSIOF interfaces configured as SPI extended from the processor and routed to a GPIO Expansion Header. The SPI interface can be operated as either master or slave. The two tables below show the signals that may be available for both MSIOF1 and MSIOF2 controllers.

MSIOF1 Signal	Baseboard Signal	Processor GPIO	Location
MSIOF1_SYNC_B	GP5_3_LCD_RESET	GP5_03	J2407.13
MSIOF1_SS1_C	GP6_21	GP6_21	J2407.18
MSIOF1_TXD_G	SD1_DAT1_V	GP3_09	J2407.19
MSIOF1_RXD_G	SD1_DAT0_V	GP3_08	J2407.21
MSIOF1_SYNC_G	SD1_CMD_V	GP3_07	J2407.22
MSIOF1_SCK_G	SD1_CLK_V	GP3_06	J2407.23
MSIOF1_SS1_G	SD1_DAT2_V	GP3_10	J2407.24
MSIOF1_SS2_G	SD1_DAT3_V	GP3_11	J2407.26
MSIOF1_SYNC_F	I2C1_SDA	GP5_24	J2407.27
MSIOF1_SCK_F	I2C1_SCL	GP5_23	J2407.28
MSIOF1_SS1_A	GP6_5/OTG_STAT1	GP6_05	J2407.29
MSIOF1_TXD_A	GP6_7/SSI_SDATA3	GP6_07	J2407.31
MSIOF1_SS2_A	GP6_6/OTG_STAT2	GP6_06	J2407.36

Table 12: MSIOF1 Signals

MSIOF2 Signal	Baseboard Signal	Processor GPIO	Location
MSIOF2_SS2_B	GP0_1	GP0_10	J2407.11
MSIOF2_SS1_B	GP0_0	GP0_00	J2407.12
MSIOF2_SYNC_A	I2C6_SDA	GP1_08	J2407.32
MSIOF2_RXD_A	M_MD20_GP1_10	GP1_10	J2407.35
MSIOF2_TXD_A	I2C6_SCL	GP1_11	J2407.38
MSIOF2_SCK_A	GP1_9	GP1_09	J2407.40

Table 13: MSIOF2 Signals

7.12 I2C

The Beacon RZ/G2 Development Kit has six Inter-Integrated Circuit (I2C) interfaces from the processor routed to the baseboard. I2C0, I2C1 and I2C6 are routed to a 40 pin GPIO header for convenient use.

- I2C0 – 40-Pin GPIO Primary Connector
- I2C1 – 40-Pin GPIO Primary Connector
- I2C2 – Baseboard Functions
- I2C3 – LVDS PWM signal and Fan PWM control
- I2C4 – SOM use only, not routed to baseboard
- I2C5 – Baseboard Functions
- I2C6 – 40-pin GPIO Primary Connector

I2C interfaces are referenced to VDDQ33 voltage at the processor. I2C level shifters are employed where 1.8V operation is necessary.

7.12.1 Address Mapping for I2C Busses

The table below shows the address mapping for all the I2C buses.

I2C Bus	Device	Ref Designator	7-Bit Address	Speed	Voltage
I2C4	Display, USB & Ethernet Clock Generator	SOM: U2439	1101010b (0x6A)	400 kHz	3.3V
I2C4	RTC	SOM: U2431	1010001b (0x51)	400 kHz	3.3V
I2C4	Secure Element	SOM: U7	1001000b (0x48)	400 kHz	3.3V
I2C4	EEPROM	SOM: U2420	1010000b (0x50)	400 kHz	3.3V
I2C4	Wi-Fi/BT GPIO Expander	SOM: U1202	0100000b (0x20)	400 kHz	3.3V
I2C4	PCIe Clock Generator (SMBus)	SOM: U1301	1101000b (0x68)	400 kHz	3.3V
I2C4	Cellular/GNNS GPIO Expander	SOM: U2422	0100001b (0x21)	400 kHz	3.3V
IIC_DVFS	DVFS0.8V Regulator	SOM: U2304	0011100b (0x1C)	400 kHz	1.8V
IIC_DVFS	DDRx1.1V Regulator	SOM: U2302	0011111b (0x1F)	400 kHz	1.8V
IIC_DVFS	VDD0.8V Regulator	SOM: U2303	0011110b (0x1E)	400 kHz	1.8V
I2C5	Audio CODEC	Baseboard: U71	0011010b (0x1A)	400 kHz	3.3V
I2C5	Audio CODEC	Baseboard: U71	1001010b (0x4A)	400 kHz	3.3V
I2C5	Audio CODEC	Baseboard: U71	1101001b (0x69)	400 kHz	3.3V
I2C5	USB Type C 2:1 Mux	Baseboard: U5035	1000111b (0x47)	400 kHz	3.3V
I2C5	GPIO Expander 1	Baseboard: U5024	1110000b (0x70)	400 kHz	3.3V
I2C2	GPIO Expander 2	Baseboard: U6	0100001b (0x21)	400 kHz	3.3V
I2C2	GPIO Expander 3	Baseboard: U5025	0100010b (0x22)	400 kHz	3.3V
I2C2	GPIO Expander 4	Baseboard: U5034	0100011b (0x23)	400 kHz	3.3V
I2C2	Audio and Ethernet Clock Generator	Baseboard: U2429	1101000b (0x6A)	400 kHz	3.3V
I2C5	LVDS Touch Connector	Baseboard: J2430	Varies on display	400 kHz	1V8
I2C2	CSI1 Camera Connector	Baseboard: J2421	Varies on camera	400 kHz	1V8
I2C5	CSI1 Camera Connector	Baseboard: J2438	Varies on camera	400 kHz	1V8

Table 14: Address Mappings for I2C Busses

7.13 PCIe

The Beacon RZ/G2 Development Kit provides two single-lane PCI Express Gen 2 functionality. Channel-0 routes to the baseboard M.2 Key B (J2414). Channel-1 routes to and M.2 Key M (J2413). Both sockets are on the backside of the baseboard.

7.13.1 PCIe M.2 Key B (J2414) Pin Mapping

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain	Notes
1	PCIE_B_CONFIG_3	PCIe Config 3	I/O	3.3V	VDD3.3V_PCIE	--
2	VDD3.3V_PCIE	PWR	--	3.3V	VDD3.3V	--
3	DGND	PWR	--	GND	--	--
4	VDD3.3V_PCIE	PWR	--	3.3V	VDD3.3V	--
5	DGND	PWR	--	GND	--	--
6	CAT6_POWER_OFFN	Full Card Power Off	I/O	3.3V	VDD3.3V	--
7	USB3HS0_DP	USB Data+	I/O	Variable	--	2
8	W_DISABLE1N	W_nDisable	I/O	3.3V	VDD3.3V	--
9	USB3HS0_DM	USB Data-	I/O	Variable	--	2
10	W_LED	LED		3.3V	VDD3.3V	--
11	DGND	PWR	--	GND	--	--
20	I2S_CLK	I2S Clock; connected to J2433.10	O	User Define	--	--
21	PCIE_CONFIG_0	PCIe Config 0	I/O	3.3V	VDD3.3V	--
22	PCM_IN	PCM_IN; connected to J2433.7	I	User Define	--	--
23	WAKE_ON_WANN	Wake-on-LAN	I/O	3.3V	VDD3.3V	--
24	NC_PCM_OUT	PCM_OUT; connected to J2433.9	O	User Define	--	--
25	DPR	Dynamic power reduction	O	1.8V/3.3V	BBD1V8/VDD3.3V_PCIE	--
26	GNSS_EN	GNSS Enable	O	3.3V	VDD3.3V	--
27	DGND	PWR	--	GND	--	--
28	PCM_SYNC	PCM data frame sync; connected to J2433.5 (R9605 10K pull-down)	I/O	User Define	--	--
29	EM06_USB3S0_RX_M	USB RX-	I	Variable	--	2
30	USIM1_RESET	SIM1 reset	I	1.8/3.0V	USIM1_VDD	--
31	EM06_USB3S0_RX_P	USB RX+	I	Variable	--	2
32	USIM1_CLK	SIM1 clock	I	1.8/3.0V	USIM1_VDD	--
33	DGND	PWR	--	GND	--	
34	USIM1_DATA	SIM1 Data	I/O	1.8/3.0V	USIM1_VDD	--

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain	Notes
35	EM06_USB3S0_TX_M	USB TX-1	O	Variable	--	2
36	USIM1_VDD	PWR	--	1.8/3.0V	--	3
37	EM06_USB3S0_TX_P	USB TX+1	O	Variable	--	2
38	**--**	--	--	--	--	--
39	DGND	PWR	--	GND	--	--
40	USIM2_DET	SIM2 insertion detection	O	1.8/3.0V	USIM2_VDD	
41	PCIE0_RX_M	PCIe RX-	I	Variable	VDDA_1V8	1
42	USIM2_DATA	SIM2 Data	I/O	1.8/3.0V	USIM2_VDD	--
43	PCIE0_RX_P	PCIe RX+	I	Variable		1
44	USIM2_CLK	SIM2 CLK	I	1.8/3.0V	USIM2_VDD	--
45	DGND	PWR	--	GND	--	--
46	USIM2_RESET	SIM2 Reset	I	1.8/3.0V	USIM2_VDD	--
47	PCIE0_TX_M	PCIe TX-	O	Variable	VDDA_1V8	1
48	USIM2_VDD	PWR	--	1.8/3.0V	--	3
49	PCIE0_TX_P	PCIe TX+	O	Variable	VDDA_1V8	1
50	CELLMOD_RESETN	PCIe nReset	I	3.3V	VDD3.3V_PCIE	--
51	DGND	PWR	--	GND	--	--
52	PCIECLKREQn	PCIe Clock nRequest	I/O	3.3V	VDD3.3V	
53	PCIE0_REFCLK_M	PCIe Clock-	O	Variable	VDDA_1V8	1
54	PCIEWAKEN	PCIe nWake	I/O	3.3V	VDD3.3V_PCIE	--
55	PCIE0_REFCLK_P	PCIe Clock+	O	Variable	VDDA_1V8	1
56	I2C_SDA_AUDIO	I2C data used for external codec; connected to J2433.1	I/O	User Define	User Define	--
57	DGND	PWR	--	GND		--
58	I2C_SCL_AUDIO	I2C clock used for external clock; connected to J2433,3	I	User Define	User Define	--
59	ANTCTL0	Antenna tuner control; connected to J2433,2	I	User Define	User Define	--
60	--	--	--	--	--	--
61	ANTCTL1	Antenna tuner control; connected to J2433,4	I	User Define	User Define	--
62		--	--	--	--	--
63	ANTCTL2	Antenna tuner control; connected to J2433,6	I	User Define	User Define	--
64	--	--	--	--	--	--

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain	Notes
65	ANTCTL3	Antenna tuner control; connected to J2433,8	I	User Define	User Define	--
66	USIM1_DET	SIM1 Detect	O	User Define	USIM1_VDD	--
67	BB_PRESETn_18	NC	--	--1.8V	--	--
68	ANT_CONFIG	NC	--	--	--	--
69	PCIE_CONFIG_1	NC	--	--	--	--
70	VDD3.3V_PCIE	PWR	--	3.3V	VDD3.3V	--
71	DGND	PWR	--	GND	--	--
72	VDD3.3V_PCIE	PWR	--	3.3V	VDD3.3V	--
73	DGND	PWR	--	GND	--	--
74	VDD3.3V_PCIE	PWR	--	3.3V	VDD3.3V	--
75	PCIE_CONFIG_2	NC	--	--	--	--

Note:
1. PCIe voltage levels follow the PCIe specification and depend on the operating speed. Please see PCI-SIG for more information.
2. USB voltage levels follow the USB specification and depend on the USB operating speed. Please see the USB Specification for more information.
3. Reference supply is provided by the PCIe Card.

Table 15: PCIe M.2 Key B (J2414) Pin Mapping

7.13.2 PCIe M.2 Key M (J2413) Pin Mapping

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain	Notes
1	SSD_CONFIG_3	PCIe Config 3	I/O	GND	--	--
2	VDD3.3V_SSD	PWR	--	3.3V	VDD3.3V	--
3	DGND	PWR	--	GND	--	--
4	VDD3.3V_SSD	PWR	--	3.3V	VDD3.3V	--
5	--	--	--	--	--	--
6	--	--	--	--	--	--
7	--	--	--	--	--	--
8	--	--	--	--	--	--
9	DGND	PWR	--	GND	--	
10	--	--	--	--	--	--
11	--	--	--	--	--	--
12	VDD3.3V_SSD	PWR		3.3V	VDD3.3V	--
13	--	--	--	--	--	--
14	VDD3.3V_SSD	PWR	--	3.3V	VDD3.3V	--
15	DGND	PWR	--	GND	--	--
16	VDD3.3V_SSD	PWR		3.3V	VDD3.3V	--
17	--	--	--	--	--	--
18	VDD3.3V_SSD	PWR		3.3V	VDD3.3V	

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain	Notes
19	--	--	--	--	--	--
20	--	--	--	--	--	--
21	SSD_CONFIG_0	PCIe Config 0	I/O	GND	--	--
22	--	--	--	--	--	--
23	--	--	--	--	--	--
24	--	--	--	--	--	--
25	--	--	--	--	--	--
26	--	--	--	--	--	--
27	DGND	PWR	--	GND	--	--
28	--	--	--	--	--	--
29	--	--	--	--	--	--
30	--	--	--	--	--	--
31	--	--	--	--	--	--
32	--	--	--	--	--	--
33	DGND	PWR	--	GND	--	
34	--	--	--	--	--	--
35	--	--	--	--	--	--
36	--	--	--	--	--	--
37	--	--	--	--	--	--
38	SSD_DEV_SLP	Device Disable	I/O	3.3V	VDD3.3V_SSD	--
39	DGND	PWR	--	GND	--	--
40	--	--	--	--	--	--
41	PCIE1_RX_M	PCIe RX-		Variable	VDDA_1V8	1
42	--	--	--	--	--	--
43	PCIE1_RX_P	PCIe RX+		Variable	VDDA_1V8	1
44	--	--	--	--	--	--
45	DGND	PWR	--	GND	--	
46	--	--	--	--	--	--
47	PCIE1_RX_M	PCIe TX-		Variable	VDDA_1V8	1
48	--	--	--	--	--	--
49	PCIE1_RX_P	PCIe TX+		Variable	VDDA_1V8	1
50	SSD_RESETN	SSD Reset	I/O	3.3V	VDD3.3V	--
51	DGND	PWR	--	GND	--	--
52	CLKREQn_R	PCIe Clock Request	I/O	3.3V	VDD3.3V_SSD	--
53	PCIE1_REFCLK_M	PCIe Clock -		Variable	VDDA_1V8	1
54	PEWAKEN_R	PCIe nWake	I/O	3.3V	VDD3.3V_SSD	--
55	PCIE1_REFCLK_P	PCIe Clock +		Variable	VDDA_1V8	1
56	--	--	--	--	--	--
57	DGND	PWR	--	GND	--	
58	--	--	--	--	--	--

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain	Notes
67	--	--	--	--	--	--
68	SUSCLK	NC	--	--	--	--
69	SSD_CONFIG_1	PCIe Config 1	I/O	GND	--	--
70	VDD3.3V_SSD	PWR	--	3.3V	VDD3.3V	--
71	DGND	PWR	--	GND	--	--
72	VDD3.3V_SSD	PWR	--	3.3V	VDD3.3V	--
73	DGND	PWR	--	GND	--	--
74	VDD3.3V_SSD	PWR	--	3.3V	VDD3.3V	--
75	SSD_CONFIG_2	PCIe Config 2	I/O	GND	--	--

Note:
1. PCIe voltage levels follow the PCIe specification and depend on the operating speed. Please see PCI-SIG for more information.

Table 16: PCIe M.2 Key M (J2413) Pin Mapping

7.14 RTC

The Beacon RZ/G2 Development Kit provides an ultra-low power real-time clock (RTC:U2431).

The RTC resides on the SOM and communicates to the processor on the I2C4 bus. The RTC receives battery backup voltage from a CR1225 coin cell battery inserted into a battery holder (X2102) on the baseboard. The baseboard also includes a shunt jumper (JP60), which is populated by default, to enable the coin cell battery to charge when the Development Kit is powered up.

7.15 SOM General Purpose I/O

The RZ/G2 processor has multiplexed GPIOs supporting various peripherals such as PWMs, SDIO, UART, SPI, RGB, and I2C. The RZ/G2 SOM incorporates many of the GPIOs into the design. The SOM extends the GPIO signals to the baseboard.

GPIO assignments usage appear in the “Signal Name” column, while the “Processor Alternate Functions” column shows what other GPIO selections would have been possible.

7.16 Expansion Headers

The Beacon RZ/G2 Development Kit provides two 40-pin headers on the baseboard for expansion, application development and test labeled J2407, and J77.

7.16.1 Primary GPIO Expansion Header

The Primary GPIO Expansion Header on the baseboard is at location J2407. The baseboard routes the GPIO signals as well as an option SDHI and I2C interfaces. These interfaces can also be configured as GPIO if desired. See Figure 1 for the location on the baseboard.

The pin mapping for the 40-pin (2x20) GPIO expansion header connector is shown below.

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain
1	BBD3.3V	3.3V logic power supply	PWR	3.3V	D3.3V_IN
2	BB_5V	5.0V Logic power supply	PWR	5.0V	BB_5V_IN
3	I2C0_SDA	I2C-0 data (3.3V levels)	I/O	3.3V	D3.3V_SOM
4	BB_5V	5.0V Logic power supply	PWR	5.0V	BB_5V_IN
5	I2C0_SCL	I2C0 clock (3.3V levels)	O	3.3V	D3.3V_SOM
6	DGND	Ground	PWR	GND	--
7	GP6_31	GPIO6_31	I/O	3.3V	D3.3V_SOM
8	GP5_02/TX0/HTX1_B	SCIF0 TX	O	3.3V	D3.3V_SOM
9	DGND	Ground	PWR	GND	--
10	GP5_01/RX0/HRX1_B	SCIF0 RX	I	3.3V	D3.3V_SOM
11	GP0_1	GPIO0_1	I/O	3.3V	D3.3V_SOM
12	GP0_0	GPIO0_1	I/O	3.3V	D3.3V_SOM
13	GP5_3_LCD_RESET	LCD_RESET	O	3.3V	D3.3V_SOM
14	DGND	Ground	PWR	GND	--
15	GP6_15	GPIO6_15	I/O	3.3V	D3.3V_SOM
16	GP6_14	GPIO6_14	I/O	3.3V	D3.3V_SOM
17	BBD3.3V	3.3V logic power supply	PWR	3.3V	D3.3V_IN
18	GP6_21	GPIO6_21	I/O	3.3V	D3.3V_SOM
19	SD1_DAT1_V	SDHI1 Data1	I/O	1.8/3.3V	VDDQVA_SD1
20	DGND	Ground	PWR	GND	--
21	SD1_DAT0_V	SDHI1 Data0	I/O	1.8/3.3V	VDDQVA_SD1
22	SD1_CMD_V	SDHI1 Command	O	1.8/3.3V	VDDQVA_SD1
23	SD1_CLK_V	SDHI1 Clock	O	1.8/3.3V	VDDQVA_SD1
24	SD1_DAT2_V	SDHI1 Data2	I/O	1.8/3.3V	VDDQVA_SD1
25	DGND	Ground	PWR	GND	--
26	SD1_DAT3_V	SDHI1 Data3	I/O	3.3V	VDDQVA_SD1
27	I2C1_SDA	I2C1 Data	I/O	3.3V	BBD3.3V
28	I2C1_SCL	I2C1 Clock	O	3.3V	BBD3.3V
29	GP6_5/OTG_STAT1	GP6_5/OTG_STAT1	I/O	3.3V	D3.3V_SOM
30	DGND	Ground	PWR	GND	--
31	GP6_7/SSI_SDATA3	GPIO Expansion P1-0	I/O	3.3V	D3.3V_SOM
32	I2C6_SDA	I2C6 Data	I/O	3.3V	D3.3V_SOM
33	I2C3_SDA	I2C3 Data	I/O	3.3V	D3.3V_SOM
34	DGND	Ground	PWR	GND	--
35	M_MD20_GP1_10	M_MD20_GP1_10	I/O	3.3V	D3.3V_SOM
36	GP6_6/OTG_STAT2	GP6_6/OTG_STAT2	I/O	3.3V	D3.3V_SOM
37	GP1_20	GPIO1_20	I/O	3.3V	D3.3V_SOM
38	I2C6_SCL	I2C6 Clock	O	3.3V	D3.3V_SOM
39	DGND	Ground	PWR	GND	--
40	GP1_9	GPIO1_9	I/O	3.3V	D3.3V_SOM

Table 17: Primary GPIO Expansion Header (J2407) Pin Mappings

7.16.2 Secondary Expansion Header

The baseboard includes a secondary GPIO Expansion Header at location J77 on the baseboard. The 40-pin header mostly contains signals for parallel RGB displays, but these signals can be configured as GPIO if desired. See Figure 1 for a picture.

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain
1	BBD3.3V	3.3V logic power supply	PWR	3.3V	D3.3V_IN
2	BB_5V	5.0V Logic power supply	PWR	5.0V	BB_5V_IN
3	DU_VSYNC	RGB VSYNC	I/O	3.3V	D3.3V_SOM
4	BB_5V	5.0V Logic power supply	PWR	5.0V	BB_5V_IN
5	DU_HSYNC	RGB HSYNC	O	3.3V	D3.3V_SOM
6	DGND	Ground	PWR	GND	--
7	M_MD6_DU_DR1	RGB RED1	O	3.3V	D3.3V_SOM
8	DU_DR5	RGB RED5	O	3.3V	D3.3V_SOM
9	DGND	Ground	PWR	GND	--
10	DU_DR4	RGB RED4	O	3.3V	D3.3V_SOM
11	DU_DB7	RGB BLUE7	O	3.3V	D3.3V_SOM
12	DU_DB6	RGB BLUE6	O	3.3V	D3.3V_SOM
13	DU_DB2	RGB BLUE2	O	3.3V	D3.3V_SOM
14	DGND	Ground	PWR	GND	--
15	DU_DB3	RGB BLUE3	O	3.3V	D3.3V_SOM
16	DU_DG0	RGB GREEN0	O	3.3V	D3.3V_SOM
17	BBD3.3V	3.3V Power supply	PWR	3.3V	D3.3V_IN
18	DU_DG5	RGB GREEN5	O	3.3V	D3.3V_SOM
19	DU_DG7	RGB GREEN7	O	3.3V	D3.3V_SOM
20	DGND	Ground	PWR	GND	--
21	DU_DG6	RGB GREEN6	I/O	3.3V	D3.3V_SOM
22	M_MD15_DU_DG1	RGB GREEN1	O	3.3V	D3.3V_SOM
23	M_MD21_DU_DG4	RGB GREEN64	O	3.3V	D3.3V_SOM
24	DU_DR6/MSIOF3_SS1_A	RGB RED6	I/O	3.3V	D3.3V_SOM
25	DGND	Ground	PWR	GND	--
26	DU_DR7/MSIOF3_SS2_A	RGB RED7	I/O	3.3V	D3.3V_SOM
27	GP6_16	GPIO6_16	I/O	3.3V	D3.3V_SOM
28	DU_CLK	RGB Clock	O	3.3V	D3.3V_SOM
29	DU_DG2	RGB GREEN2	O	3.3V	D3.3V_SOM
30	DGND	Ground	PWR	GND	--
31	DU_DG3	RGB GREEN3	O	3.3V	D3.3V_SOM
32	DU_DB0	RGB BLUE0	O	3.3V	D3.3V_SOM
33	DU_DB1	RGB BLUE1	O	3.3V	D3.3V_SOM
34	DGND	Ground	PWR	GND	--
35	DU_DR2	RGB RED2	O	3.3V	D3.3V_SOM
36	DU_DB4	RGB BLUE4	O	3.3V	D3.3V_SOM
37	DU_DB5	RGB BLUE4	O	3.3V	D3.3V_SOM
38	DU_DR3	RGB RED2	O	3.3V	D3.3V_SOM
39	DGND	Ground	PWR	GND	--
40	DU_DR0	RGB RED0	O	3.3V	D3.3V_SOM

Table 18: Secondary GPIO Expansion Header (J77) Pin Mappings

7.17 User Buttons

The RZ/G2 baseboard provides user buttons. The functionality of each user button is outlined in the table below.

Button	Switch Type	Signal Name	Function
S29	Tactile SPST, Momentary	PRESETn_18	System Reset
S19	Tactile SPST, Momentary	GP4_06	Up
S20	Tactile SPST, Momentary	GP3_13	Left
S21	Tactile SPST, Momentary	GP5_17	Down
S22	Tactile SPST, Momentary	GP5_20	Right
S23	Tactile SPST, Momentary	GP5_22	Center
S28	Tactile SPST, Momentary	RSTBN	SOM Power On/Off

Table 19: Baseboard User Buttons

7.18 LEDs

The RZ/G2 baseboard provides Light Emitting Diodes (LEDs).

Reference	Description	Color
D47	SOM RESET LED	Red
D2419	Baseboard Reset LED	Red
D2407	PRESETOUTn LED	Green
D46	SOM Power	Green
D2420	Baseboard Power	Green
D6	LED0, GP0_4	Green
D7	LED1, GP7_0	Green
D8	LED2, GP7_1	Green
D9	LED3, GP7_3	Green
D28	U5005 - FTDI_nRXLED1	Yellow
D2417	U5005 - FTDI_nTXLED1	Green
D29	U5005 - FTDI_nRXLED2	Yellow
D2418	U5005 - FTDI_nTXLED2	Green
D32	W_LED	Green

Table 20: Baseboard LEDs

8 System Integration

8.1 Boot Device Selection

The Baseboard provides an 8-Bit DIP Switch (SPDT) for the Boot Mode Selection at location S26. The Boot Mode switches to determine the boot source of the RZ/G2 processors. The boot source can boot from QSPI Flash, eMMC or a SCIF serial download. When booting from QSPI or eMMC, the Linux Kernel can be loaded and executed from eMMC, SD Card, USB or Ethernet. The Beacon RZ/G2 SOM provides access to four boot device pins, MD1 - MD4, through the off-board connectors. The MD1-4 pins choose which device from which the boot ROM will load the boot loader.

The baseboard boot mode switches present a logical 0 when in the minus (-) position and logical 1 when in the plus (+) position. The switches may also be kept in the disconnected (O) position, in which case pullup or pulldown resistors on the SOM will determine the initial state, which is equivalent to the boot mode switch options shown in the figure below. S26:5-8 should all remain in their default position.

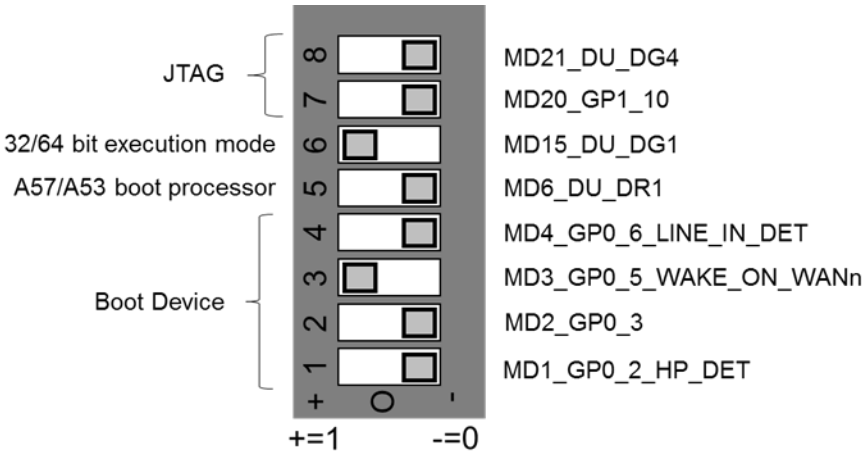

Figure 17: Baseboard Boot Mode Switches (S26)

Ref Designator	Signal	RZ/G2 Pin	Notes
S26.1	MD1	AJ2	—
S26.2	MD2	AJ1	—
S26.3	MD3	AH5	—
S26.4	MD4	AH4	—

Table 21: RZ/G2 Boot Device Pins

Table 22: RZ/G2 Boot Device Settings below describes the available boot modes on the RZ/G2. Please refer to "Section 6.1.2" of *RZ/G2 Applications Processor Reference Manual* for further details. Note that the MD pins are sampled on the rising edge of the nPOR pin. The S26 switch selector has three states, +, -, and floating. For the table below ensure the switches are fully pushed to the + or – configuration and not left in the tri-state/middle position.

S26	Mode Pin	QSPI	eMMC	SCIF Serial
1	MD01	-	+	+
2	MD02	-	-	+
3	MD03	+	+	+
4	MD04	-	+	+
5	MD06	-	-	-
6	MD15	+	+	+
7	MD20	-	-	-
8	MD21	-	-	-

Table 22: RZ/G2 Boot Device Settings

8.2 Boot Mode Isolator

The Baseboard provides an isolator component (U2434) that isolates the mode pins from other circuits on the Baseboard until the states of the boot mode switches have been sampled.

Parameter	Detail
Manufacturer Part Number	SN74CBTLV3245ARGYR
Manufacturer	Texas Instruments
Description	IC OCTAL FET BUS SW LV 20-VQFN
Type / Circuit	Bus Switch / 8 x 1:1
Voltage - Supply	2.3V to 3.6V
Package / Case	20-VFQFN Exposed Pad / Surface Mount

Table 23: Boot Mode Isolator Specification

8.3 Resets

8.3.1 System Reset

The RZ/G2 baseboard drives System Reset (PRESETn_18) via the S29 Button Switch. The S29 Button Switch is connected to the power button input (PRESET#) of the SoC and it connects to the QSPI and eMMC to reset them when S29 is pressed. System reset is considered the main reset for the development kit.

8.4 Interrupts

All GPIOs can be configured as an interrupt source. Both edge-sensitive and level-sensitive interrupts are supported. Refer to sections 10.2 and 10.3 of the RZ/G Series 2nd Generation User's Manual Hardware for more detailed information on interrupt sources.

The RZ/G2 processor's internal thermal sensor and voltage monitor can also be configured as interrupt sources. For more information, refer to section 15 of the RZ/G2 Hardware Manual.

Sections 18-20 of the RZ/G2 Hardware Manual provide details on the operation of the Interrupt Controllers.

8.5 JTAG Debug Interface

The RZ/G2 SOM routes the JTAG interface to the host off-board connectors. These signals are routed to a JTAG header (J2424) on the baseboard. See Figure 1: Baseboard (Front Side) for a picture which includes the JTAG header, near the microSD Card socket. The pin mapping for the 10-pin (2x5) JTAG header is shown in the table below.

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain
1	1.8V	JTAG Power	PWR	1.8V	BBD1V8
2	TMS_18	JTAG_TMS	I	1.8V	BBD1V8
3	DGND	Ground	PWR	GND	--
4	TCK_18	JTAG_TCK	I	1.8V	D1.8V_SOM
5	DGND	Ground	PWR	GND	--
6	TDO_18	JTAG_TDO	O	1.8V	BBD1V8
7	No Connect (default)	No Connect (default)	--	--	--
8	TDI_18	JTAG_TDI	I	1.8V	BBD1V8
9	Ground (default)	Ground (default) or BBD1V8 when S31 is set to TRSTn_H_18.	PWR	GND	--
10	JTAG_TRSTN	JTAG_TRSTN	O	1.8V	D3.3V_SOM

Table 24: JTAG Connector (J2424) Pin Mappings

8.6 Power Supplies

8.6.1 Baseboard Power Supply Structure

The entire Beacon RZ/G2 Development Kit is powered from a single connector (J53) on the baseboard. Users must use the supply provided originally with the development kit. See Figure 1 for a picture which includes the power-in jack (J53) flagged on the upper right side. Just below the power connector is the Main Power On-Off button (S28).

A block diagram of the baseboard power structure is shown in the figure below.

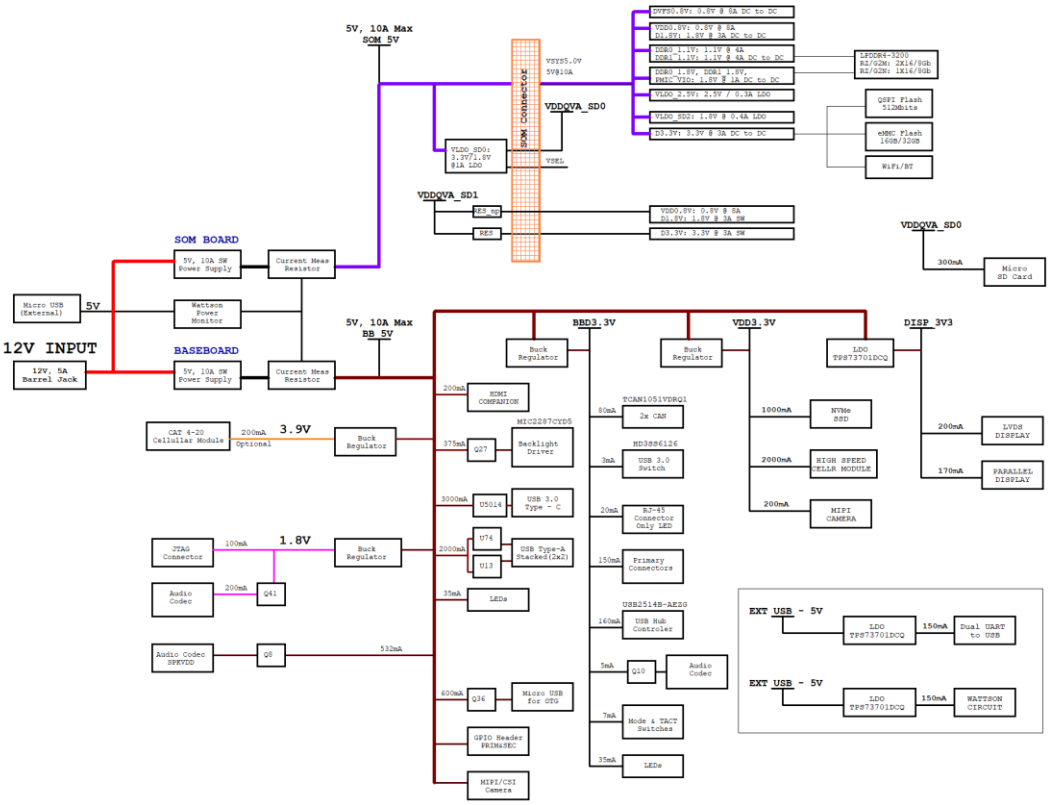

Figure 18: Baseboard Power Structure Block Diagram

8.6.1.1 SOM5V

The RZ/G2 baseboard supplies power to the SOM from a buck regulator connected to the 12V_IN supply connecting to the power jack, J53. This supply is monitored by Wattson and listed as “SOM_5V_IN”. The SOM_5V power can be measured with Wattson using the power monitor 0 through power measurement resistors R9599, R2518, R9597, and R9598.

8.6.1.1.1 BB_5V

The RZ/G2 baseboard power supply, BB_5V_IN, comes from a buck regulator connected to the 12V_IN supply connecting to the power jack, J53. This supply is monitored by Wattson and listed as “SOM_5V_IN”. The BB_5V power can be measured with Wattson using the power monitor 1 through power measurement resistors R9911, R2522, R9912, and R9913.

8.6.1.1.2 VCC_3V9

The VCC_3V8_IN supply is regulated by a synchronous step-down regulator (U15). BB_5V is the input supply for the D3.3V_IN regulator. D3.3V_IN can be accessed on the baseboard on the test point called TP_D3V3. This supply is monitored by Wattson and listed as “VCC_3V9_IN”. The VCC_3V9 power can be measured with Wattson using power monitor 6 through power measurement resistor R160. This supply is used on the baseboard for VCC_3V9 and it is the primary power supply for the baseboard 3.9V rail powering the PCIe interface.

8.6.1.1.3 D3.3V_IN

The D3.3V_IN supply is regulated by a synchronous step-down regulator (U5011). BB_5V is the input supply for the D3.3V_IN regulator. D3.3V_IN can be accessed on the baseboard on the test point called TP_D3V3. This supply is monitored by Wattson and listed as D3.3V_IN. The D3.3V_IN power can be measured with Wattson using power monitor 5 through power measurement resistor R9812. This supply is used on the baseboard for BBD3.3V and it is the primary power supply for the baseboard 3.3V rail.

8.6.1.1.4 VDD3.3V_IN

The VDD3.3V_IN supply is regulated by a synchronous step-down regulator (U2307) and controlled using the PWR_GOOD_BB_5V signal. BB_5V is the input supply for the VDD3.3V_IN regulator. VDD3.3V_IN can be accessed on the baseboard on the test point called TP_VDD3V3. This supply is monitored by Wattson and listed as “VDD3.3V_IN”. The VDD3.3V_IN power can be measured with Wattson using power monitor 2 through power measurement resistor R159. This supply is used on the baseboard for VDD3.3V and it is the primary power supply for the level-shifters and reference voltages of 3.3V.

8.6.1.1.5 DISP_3V3_IN

The VDD3.3V_IN supply is regulated by an LDO regulator (U5013) and controlled using the PWR_GOOD_BB_5V signal. BB_5V is the input supply for the DISP_3V3_IN regulator. This supply is monitored by Wattson and listed as “DISP_3V3_IN”. The DISP_3V3_IN power can be measured with Wattson using power monitor 4 through power measurement resistor R9810. This supply is used on the baseboard for DISP_3V3 and it is the primary power of the LVDS display.

8.6.1.1.6 BBD1V8

The 1V8_IN supply is regulated by a synchronous step-down regulator (U2411) and controlled using PWR_GOOD_BB_5V signal. BB_5V is the input supply for the 1V8 regulator. This supply is monitored by Wattson and listed as “1V8_IN”. This supply is monitor by Wattson monitor 3 through power measurement resistor R9811. This is the primary supply for any 1.8V on the baseboard. The 1V8 power can be accessed on the baseboard at locations J29 (pins 10.

8.6.2 VBACKUP

The baseboard provides a VBAK_RTC rail to power the PCF85263ATT RTC on the SOM when SOM_5V is not present. VBAK_RTC is derived from a coin cell battery (3.0V) on the baseboard. The VBAK_RTC domain can be accessed on the baseboard at location JP60.

9 Electrical Specification

9.1 Absolute Maximum Ratings

The Beacon RZ/G2 Development Kit absolute maximum specifications are shown in the table below.

Parameter	Symbol	Min (V)	Max (V)
DC Main System External Supply	J53	VSS-0.3	13.2
RTC Backup Battery Voltage	VBAK_RTC	VSS-0.3	3.3

*Table **25**: Absolute Maximum Ratings*

NOTE: These stress ratings are only for transient conditions. Operation at or beyond absolute maximum rating conditions may affect reliability and cause permanent damage to the RZ/G2 SOM and baseboard.

9.2 Recommended Operating Conditions

The Beacon RZ/G2 Development Kit temperature specifications are shown in the table below.

Parameter	Symbol	Min (V)	Typ (V)	Max (V)	Units
DC Main System External Supply	J38	10.8	12.0	13.2	V
RTC Backup Battery Voltage	VBAK_RTC	0.9[6]	3.0	3.3	V
Operating Temperature	--	0	--	70	°C
Storage Temperature	--	0	--	70	°C

*Table **26**: Recommended Operating Conditions*

[6] For reliable oscillator start-up at power-on use VBACKUP_IN (PCF85263A.VDD) greater than 1.2 V. If powered up at 0.9 V the oscillator will start but it might be a bit slow, especially if at high temperature. Normally the power supply is not 0.9 V at start-up and only comes at the end of battery discharge. VDD min of 0.9 V is specified so that the customer can calculate how large a battery or capacitor they need for their application. VDD min of 1.2 V or greater is needed to ensure speedy oscillator start-up time. The RTC was tested by NXP at 1.8V for 400 KHz I2C operation.

10 Environment

10.1 ESD Considerations

The RZ/G2 SOM extends and integrates with the baseboard functionality and was not designed to be hot-plugged or have external ports exposed to direct end user access. The RZ/G2 SOMs are static sensitive devices. Care should be taken when handling to avoid contact with charged persons, devices or surfaces.

The RZ/G2 SOM does not incorporate any ESD protection and therefore relies on the baseboard to provide the protection at the point of contact for any externally accessible connectors or access points that directly route to the SOM.

11 Baseboard Connectors - Pin Descriptions & Functions

The tables in this section describe the signals as seen on the connectors on the baseboard that interface to the Beacon EmbeddedWorks SOMs.

11.1 J1 Baseboard Connector

J1 Pin#	Signal Name	BGA Ball#	Processor Alternate Functions	I/O	Voltage (V)	Signal Description
J1-1	DGND	--	--	--	GND	Digital Ground
J1-2	DGND	--	--	--	GND	Digital Ground
J1-3	DGND	--	--	--	GND	Digital Ground
J1-4	DGND	--	--	--	GND	Digital Ground
J1-5	DGND	--	--	--	GND	Digital Ground
J1-6	DGND	--	--	--	GND	Digital Ground
J1-7	DGND	--	--	--	GND	Digital Ground
J1-8	DGND	--	--	--	GND	Digital Ground
J1-9	DGND	--	--	--	GND	Digital Ground
J1-10	DGND	--	--	--	GND	Digital Ground
J1-11	HDMI0_TMDSDATAP2	AN17	HDMI0_TMDSDATAP2	I	1.8V	HDMI_TX2 P. 100-ohm differential pair with HDMI_TX2_N.
J1-12	Reserved (HDMI1)	--	--	--	--	Reserved for future use. Do not connect.
J1-13	HDMI0_TMDSDATAN2	AM17	HDMI0_TMDSDATAN2	I	1.8V	HDMI_TX2 N. 100-ohm differential pair with HDMI_TX2_P.
J1-14	Reserved (HDMI1)	--	--	--	--	Reserved for future use. Do not connect.
J1-15	DGND	--	--	--	GND	Digital Ground
J1-16	DGND	--	--	--	GND	Digital Ground

J1 Pin#	Signal Name	BGA Ball#	Processor Alternate Functions	I/O	Voltage (V)	Signal Description
J1-17	HDMI0_TMDSDATAP1	AR16	HDMI0_TMDSDATAP1	I	1.8V	HDMI_TX1 P. 100-ohm differential pair with HDMI_TX1_N.
J1-18	Reserved (HDMI1)	--	--	--	--	Reserved for future use. Do not connect.
J1-19	HDMI0_TMDSDATAN1	AP16	HDMI0_TMDSDATAN1	I	1.8V	HDMI_TX1 N. 100-ohm differential pair with HDMI_TX1_P.
J1-20	Reserved (HDMI1)	--	--	--	--	Reserved for future use. Do not connect.
J1-21	DGND	--	--	--	GND	Digital Ground
J1-22	DGND	--	--	--	GND	Digital Ground
J1-23	HDMI0_TMDSDATAP0	AN15	HDMI0_TMDSDATAP0	I	1.8V	HDMI_TX0 P. 100-ohm differential pair with HDMI_TX0_N.
J1-24	Reserved (HDMI1)	--	--	--	--	Reserved for future use. Do not connect.
J1-25	HDMI0_TMDSDATAN0	AM15	HDMI0_TMDSDATAN0	I	1.8V	HDMI_TX0 N. 100-ohm differential pair with HDMI_TX0_P.
J1-26	Reserved (HDMI1)	--	--	--	--	Reserved for future use. Do not connect.
J1-27	DGND	--	--	--	GND	Digital Ground
J1-28	DGND	--	--	--	GND	Digital Ground
J1-29	HDMI0_TMDSCLKP	AR14	HDMI0_TMDSCLKP	I	1.8V	HDMI_CLK_P. 100-ohm differential pair with HDMI_CLK_N.
J1-30	Reserved (HDMI1)	--	--	--	--	Reserved for future use. Do not connect.
J1-31	HDMI0_TMDSCLKN	AP14	HDMI0_TMDSCLKN	I	1.8V	HDMI_CLK_N. 100-ohm differential pair with HDMI_CLK_P.
J1-32	Reserved (HDMI1)	--	--	--	--	Reserved for future use. Do not connect.
J1-33	DGND	--	--	--	GND	Digital Ground

J1 Pin#	Signal Name	BGA Ball#	Processor Alternate Functions	I/O	Voltage (V)	Signal Description
J1-34	DGND	--	--	--	GND	Digital Ground
J1-35	HDMI0_SCL	AK13	HDMI0_SCL	I	1.8V	HDMI0 I2C Clock
J1-36	Reserved (HDMI1)	--	--	--	--	Reserved for future use. Do not connect.
J1-37	HDMI0_SDA	AK14	HDMI0_SDA	IO	1.8V	HDMI0 I2C Data
J1-38	Reserved (HDMI1)	--	--	--	--	Reserved for future use. Do not connect.
J1-39	DGND	--	--	--	GND	Digital Ground
J1-40	DGND	--	--	--	GND	Digital Ground
J1-41	HDMI0_CEC	AK12	GP7_02	IO	3.3V	GPIO signal
J1-42	Reserved (HDMI1)	--	--	--	--	Reserved for future use. Do not connect.
J1-43	HDMI0_HPD	AL14	HDMI0_HPD	I	--	HDMI0 Hot Plug Detect
J1-44	Reserved (HDMI1)	--	--	--	--	Reserved for future use. Do not connect.
J1-45	DGND	--	--	--	GND	Digital Ground
J1-46	DGND	--	--	--	GND	Digital Ground
J1-47	LVDS0_CH0_P	AN13	LVDS0_CH0_P	I	1.8V	LVDS0 CLK P. 100-ohm differential pair with LVDS0_CLK_N.
J1-48	ETH_TRX0_P	--	--	IO	Variable (See Note 1)	ETH_TRX0_P. 100-ohm differential pair with ETH_TRX0_N.
J1-49	LVDS0_CH0_N	AM13	LVDS0_CH0_N	I	1.8V	LVDS0 CLK N. 100-ohm differential pair with LVDS0_CLK_P.
J1-50	ETH_TRX0_N	--	--	IO	Variable (See Note 1)	ETH_TRX0_N. 100-ohm differential pair with ETH_TRX0_P.
J1-51	DGND	--	--	--	GND	Digital Ground
J1-52	DGND	--	--	--	GND	Digital Ground

J1 Pin#	Signal Name	BGA Ball#	Processor Alternate Functions	I/O	Voltage (V)	Signal Description
J1-53	LVDS0_CH1_P	AR12	LVDS0_CH1_P	I	1.8V	LVDS0 TX1_P. 100-ohm differential pair with LVDS0_TX1_N.
J1-54	ETH_TRX1_P	--	--	IO	Variable (See Note 1)	ETH_TRX1_P. 100-ohm differential pair with ETH_TRX1_h.
J1-55	LVDS0_CH1_N	AP12	LVDS0_CH1_N	I	1.8V	LVDS0 TX1_N. 100-ohm differential pair with LVDS0_TX1_P.
J1-56	ETH_TRX1_N	--	--	IO	Variable (See Note 1)	ETH_TRX1_N. 100-ohm differential pair with ETH_TRX1_P.
J1-57	DGND	--	--	--	GND	Digital Ground
J1-58	DGND	--	--	--	GND	Digital Ground
J1-59	LVDS0_CH2_P	AR11	LVDS0_CH2_P	I	1.8V	LVDS0 TX2_P. 100-ohm differential pair with LVDS0_TX2_N.
J1-60	ETH_TRX2_P	--	--	IO	Variable (See Note 1)	ETH_TRX2_P. 100-ohm differential pair with ETH_TRX2_N.
J1-61	LVDS0_CH2_N	AP11	LVDS0_CH2_N	I	1.8V	LVDS0 TX2_N. 100-ohm differential pair with LVDS0_TX2_P.
J1-62	ETH_TRX2_N	--	--	IO	Variable (See Note 1)	ETH_TRX2_N. 100-ohm differential pair with ETH_TRX0_P.
J1-63	DGND	--	--	--	GND	Digital Ground
J1-64	DGND	--	--	--	GND	Digital Ground
J1-65	LVDS0_CH3_P	AN9	LVDS0_CH3_P	I	1.8V	LVDS0 TX3_P. 100-ohm differential pair with LVDS0_TX3_N.
J1-66	ETH_TRX3_P	--	--	IO	Variable (See Note 1)	ETH_TRX2_P. 100-ohm differential pair with ETH_TRX2_N.

J1 Pin#	Signal Name	BGA Ball#	Processor Alternate Functions	I/O	Voltage (V)	Signal Description
J1-67	LVDS0_CH3_N	AM9	LVDS0_CH3_N	I	1.8V	LVDS0 TX3_N. 100-ohm differential pair with LVDS0_TX3_P.
J1-68	ETH_TRX3_N	--	--	IO	Variable (See Note 1)	ETH_TRX3_N. 100-ohm differential pair with ETH_TRX3_P.
J1-69	DGND	--	--	--	GND	Digital Ground
J1-70	DGND	--	--	--	GND	Digital Ground
J1-71	LVDS0_CLK_P	AN10	LVDS0_CLK_P	I	1.8V	LVDS0 CLK_P. 100-ohm differential pair with LVDS0_CLK_N.
J1-72	Reserved (ENET_XTLI)	--	--	--	--	Reserved for future use. Do not connect.
J1-73	LVDS0_CLK_N	AM10	LVDS0_CLK_N	I	1.8V	LVDS0 CLK_N. 100-ohm differential pair with LVDS0_CLK_P.
J1-74	Reserved (LED_LINK10_100)	--	--	--	--	Reserved for future use. Do not connect.
J1-75	DGND	--	--	--	GND	Digital Ground
J1-76	LED_LINK	--	--	I	1.8V	LED input for link. Active high. This signal has a 10k ohm pull-up. Note: This is a 1.8V signal and pulled up with R10264 to 3.3V (BBD3.3V) to drive an LED.
J1-77	GP5_3	AA35	GP5_03/CTS0#/HCTS1#_B/MSIOF1_SYNC_B/AUDIO_CLKOUT_C	I	3.3V	LCD Reset
J1-78	LED_ACT	--	--	I	1.8V	LED input for 10/100/1000 BASE-T activity. Active high. This signal has a 10k ohm pull-up. Note: This is a 1.8V signal and pulled up with R10261 to 3.3V (BBD3.3V) to drive an LED.
J1-79	GP6_12	AF34	GP6_12/SSI_WS5	O	3.3V	Power Button Sense
J1-80	DGND	--	--	--	GND	Digital Ground
J1-81	PWM0	W6	GP2_06/PWM0/AVB_AVTP_PPS/VI4_DATA6_B	I	3.3V	RGB Backlight
J1-82	--	--	--	--	--	Reserved for future use. Do not connect.

J1 Pin#	Signal Name	BGA Ball#	Processor Alternate Functions	I/O	Voltage (V)	Signal Description
J1-83	GP5_9	AB35	GP5_09/SCK2/SCIF_CLK_B/MSIOF1_SCK_B	O	3.3V	Touchscreen Int
J1-84	--	--	--	--	--	Reserved for future use. Do not connect.
J1-85	GP6_4	AD31	GP6_04/SSI_SDATA2_A/SSI_SCK1_B	O	3.3V	USB-C Mux Int
J1-86	DGND	--	--	--	GND	Digital Ground
J1-87	USB3HS0_ID	AN27	USB3HS0_ID	O	3.3V	USB3 ID
J1-88	USB3S0_RX_P	AR30	USB3S0_RX_P	O	Variable (See Note 2)	USB SS RX+. 90-ohm differential pair with USB SS RX-.
J1-89	ENET_PPS	--	--	--	--	Reserved for future use. Do not connect.
J1-90	USB3S0_RX_M	AP30	USB3S0_RX_M	O	Variable (See Note 2)	USB SS RX-. 90-ohm differential pair with USB SS RX+.
J1-91	DGND	--	--	--	GND	Digital Ground
J1-92	DGND	--	--	--	GND	Digital Ground
J1-93	ENET_CLK_25M	--	--	--	--	Reserved for future use. Do not connect.
J1-94	USB3S0_TX_P	AR28	USB3S0_TX_P	I	Variable (See Note 2)	USB SS TX+. 90-ohm differential pair with USB SS TX-.
J1-95	DGND	--	--	--	GND	Digital Ground
J1-96	USB3S0_TX_M	AP28	USB3S0_TX_M	I	Variable (See Note 2)	USB SS TX-. 90-ohm differential pair with USB SS TX+.
J1-97	MD1/GP0_2	AJ2	MD1/GP0_02/MSIOF3_RXD_A/VI4_DATA18/VI5_DATA2	O	3.3V	Headphone Detect
J1-98	DGND	--	--	--	GND	Digital Ground
J1-99	MD4/GP0_6	AH4	MD4/GP0_06/MSIOF2_RXD_B/VI4_DATA22/VI5_DATA6	O	3.3V	Line-In Detect
J1-100	USB3HS0_DP	AR26	USB3HS0_DP	I/O	Variable (See Note 2)	USB-C D+. 90-ohm differential pair with USB-C D-.
J1-101	MD3/GP0_5	AH5	MD3/GP0_05/MSIOF2_SYNC_B/VI4_DATA21/VI5_DATA5	O	3.3V	Boot Mode / Wake on WANn

J1 Pin#	Signal Name	BGA Ball#	Processor Alternate Functions	I/O	Voltage (V)	Signal Description
J1-102	USB3HS0_DM	AP26	USB3HS0_DM	I/O	Variable (See Note 2)	USB-C D-. 90-ohm differential pair with USB-C D+.
J1-103	MD2/GP0_3	AJ1	MD2/GP0_03/MSIOF3_TXD_A/VI4_DATA19/VI5_DATA3	O	3.3V	Boot Mode
J1-104	DGND	--	--	--	GND	Digital Ground
J1-105	DGND	--	--	--	GND	Digital Ground
J1-106	USB3HS0_VBUS	AM26	USB3HS0_VBUS	O	-	USB-C Power Feedback
J1-107	CSI1_DATAP1	AN2	CSI1_DATAP1	O	Variable (See Note 3)	Camera 1 D1+, 100-ohm differential pair with Camera 1 D1-.
J1-108	USB30_PWEN	AJ33	GP6_28/USB30_PWEN/AUDIO_CLKOUT_B/SSI_SCK2_B/TCLK2_B/TPU0TO0/HRTS2#_C	I	3.3V	USB30 Enable
J1-109	CSI1_DATAN1	AN1	CSI1_DATAN1	O	Variable (See Note 3)	Camera 1 D1-, 100-ohm differential pair with Camera 1 D1+.
J1-110	USB30_OVC	AH30	GP6_29/USB30_OVC/AUDIO_CLKOUT1_B/SSI_WS2_B/TPU0TO1	O	3.3V	USB30 Over Current
J1-111	DGND	--	--	--	GND	Digital Ground
J1-112	DGND	--	--	--	GND	Digital Ground
J1-113	CSI1_DATAP0	AR2	CSI1_DATAP0	O	Variable (See Note 3)	Camera 1 D0+, 100-ohm differential pair with Camera 1 D0-.
J1-114	CAN0_TX	AB2	GP1_23/RD#/MSIOF3_SYNC_D/RX3_A/HRX3_A/CAN0_TX_A/CANFD0_TX_A	I	3.3V	CAN0 Tx
J1-115	CSI1_DATAN0	AP2	CSI1_DATAN0	O	Variable (See Note 3)	Camera 1 D0-, 100-ohm differential pair with Camera 1 D0+.
J1-116	CAN0_RX	AA6	GP1_24/RD/WR#/MSIOF3_RXD_D/TX3_A/HTX3_A/CAN0_RX_A/CANFD0_RX_A	O	3.3V	CAN0 Rx
J1-117	DGND	--	--	--	GND	Digital Ground
J1-118	DGND	--	--	--	GND	Digital Ground
J1-119	CSI1_CLKP	AN4	CSI1_CLKP	O	Variable (See Note 3)	Camera 1 CLK+, 100-ohm differential pair with Camera 1 CLK-.
J1-120	CAN1_TX	AB6	GP1_22/BS#/MSIOF3_SCK_D/SCK3/HSCK3/CAN1_TX/CANFD1_TX	I	3.3V	CAN1 Tx

J1 Pin#	Signal Name	BGA Ball#	Processor Alternate Functions	I/O	Voltage (V)	Signal Description
J1-121	CSI1_CLKN	AM4	CSI1_CLKN	O	Variable (See Note 3)	Camera 1 CLK-, 100-ohm differential pair with Camera 1 CLK+.
J1-122	CAN1_RX	AA2	GP1_26/WE1#/MSIOF3_SS1_D/RTS3#/HRTS3#/SDA6_B/CAN1_RX/CANFD1_RX	O	3.3V	CAN1 Rx
J1-123	DGND	--	--	--	GND	Digital Ground
J1-124	DGND	--	--	--	GND	Digital Ground
J1-125	CSI0_DATAP3	AR3	CSI0_DATAP3	O	Variable (See Note 3)	Camera 0 D3+, 100-ohm differential pair with Camera 0 D3-.
J1-126	Reserved (CSI2)	--	--	--	--	Reserved for future use. Do not connect.
J1-127	CSI0_DATAN3	AP3	CSI0_DATAN3	O	Variable (See Note 3)	Camera 0 D3-, 100-ohm differential pair with Camera 0 D3+.
J1-128	Reserved (CSI2)	--	--	--	--	Reserved for future use. Do not connect.
J1-129	DGND	--	--	--	GND	Digital Ground
J1-130	DGND	--	--	--	GND	Digital Ground
J1-131	CSI0_DATAP2	AR5	CSI0_DATAP2	O	Variable (See Note 3)	Camera 0 D2+, 100-ohm differential pair with Camera 0 D2-.
J1-132	Reserved (CSI2)	--	--	--	--	Reserved for future use. Do not connect.
J1-133	CSI0_DATAN2	AP5	CSI0_DATAN2	O	Variable (See Note 3)	Camera 0 D2-, 100-ohm differential pair with Camera 0 D2+.
J1-134	Reserved (CSI2)	--	--	--	--	Reserved for future use. Do not connect.
J1-135	DGND	--	--	--	GND	Digital Ground
J1-136	DGND	--	--	--	GND	Digital Ground
J1-137	CSI0_DATAP1	AR6	CSI0_DATAP1	O	Variable (See Note 3)	Camera 0 D1+, 100-ohm differential pair with Camera 0 D1-.

J1 Pin#	Signal Name	BGA Ball#	Processor Alternate Functions	I/O	Voltage (V)	Signal Description
J1-138	Reserved (CSI2)	--	--	--	--	Reserved for future use. Do not connect.
J1-139	CSI0_DATAN1	AP6	CSI0_DATAN1	O	Variable (See Note 3)	Camera 0 D1-, 100-ohm differential pair with Camera 0 D1+.
J1-140	Reserved (CSI2)	--	--	--	--	Reserved for future use. Do not connect.
J1-141	DGND	--	--	--	GND	Digital Ground
J1-142	DGND	--	--	--	GND	Digital Ground
J1-143	CSI0_DATAP0	AR8	CSI0_DATAP0	O	Variable (See Note 3)	Camera 0 D0+, 100-ohm differential pair with Camera 0 D0-.
J1-144	Reserved (CSI2)	--	--	--	--	Reserved for future use. Do not connect.
J1-145	CSI0_DATAN0	AP8	CSI0_DATAN0	O	Variable (See Note 3)	Camera 0 D0-, 100-ohm differential pair with Camera 0 D0+.
J1-146	Reserved (CSI2)	--	--	--	--	Reserved for future use. Do not connect.
J1-147	DGND	--	--	--	GND	Digital Ground
J1-148	DGND	--	--	--	GND	Digital Ground
J1-149	CSI0_CLKP	AN7	CSI0_CLKP	O	Variable (See Note 3)	Camera 0 CLK+, 100-ohm differential pair with Camera 0 CLK-.
J1-150	Reserved (CSI2)	--	--	--	--	Reserved for future use. Do not connect.
J1-151	CSI0_CLKN	AM7	CSI0_CLKN	O	Variable (See Note 3)	Camera 0 CLK-, 100-ohm differential pair with Camera 0 CLK+.
J1-152	Reserved (CSI2)	--	--	--	--	Reserved for future use. Do not connect.
J1-153	DGND	--	--	--	GND	Digital Ground
J1-154	DGND	--	--	--	GND	Digital Ground

J1 Pin#	Signal Name	BGA Ball#	Processor Alternate Functions	I/O	Voltage (V)	Signal Description
J1-155	PCIE0_TX_P	AP22	PCIE0_TX_P	I	Variable (See Note 4)	PCIE 0 TX+. 85-ohm differential pair with PCIE 0 TX-.
J1-156	PCIE1_TX_P	AP18	PCIE1_TX_P	I	Variable (See Note 4)	PCIE 1 TX+. 85-ohm differential pair with PCIE 1 TX-.
J1-157	PCIE0_TX_M	AR22	PCIE0_TX_M	I	Variable (See Note 4)	PCIE 0 TX-. 85-ohm differential pair with PCIE 0 TX+.
J1-158	PCIE1_TX_M	AR18	PCIE1_TX_M	I	Variable (See Note 4)	PCIE 1 TX-. 85-ohm differential pair with PCIE 1 TX+.
J1-159	DGND	--	--	--	GND	Digital Ground
J1-160	DGND	--	--	--	GND	Digital Ground
J1-161	PCIE0_RX_P	AP24	PCIE0_RX_P	O	Variable (See Note 4)	PCIE 0 RX+. 85-ohm differential pair with PCIE 0 RX-.
J1-162	PCIE1_RX_P	AP20	PCIE1_RX_P	O	Variable (See Note 4)	PCIE 1 RX+. 85-ohm differential pair with PCIE 1 RX-.
J1-163	PCIE0_RX_M	AR24	PCIE0_RX_M	O	Variable (See Note 4)	PCIE 0 RX-. 85-ohm differential pair with PCIE 0 RX+.
J1-164	PCIE1_RX_M	AR20	PCIE1_RX_M	O	Variable (See Note 4)	PCIE 1 RX-. 85-ohm differential pair with PCIE 1 RX+.
J1-165	DGND	--	--	--	GND	Digital Ground
J1-166	DGND	--	--	--	GND	Digital Ground
J1-167	PCIE0_REFCLK_P	--	--	I	Variable (See Note 4)	PCIE 0 REF CLK+. 85-ohm differential pair with PCIE 0 REF CLK-.
J1-168	PCIE1_REFCLK_P	--	--	I	Variable (See Note 4)	PCIE 1REF CLK+. 85-ohm differential pair with PCIE 1 REF CLK-.

J1 Pin#	Signal Name	BGA Ball#	Processor Alternate Functions	I/O	Voltage (V)	Signal Description
J1-169	PCIE0_REFCLK_M	--	--	I	Variable (See Note 4)	PCIE 0 REF CLK-. 85-ohm differential pair with PCIE 0 REF CLK+.
J1-170	PCIE1_REFCLK_M	--	--	I	Variable (See Note 4)	PCIE 1 REF CLK-. 85-ohm differential pair with PCIE 1 REF CLK+.
J1-171	DGND	--	--	--	GND	Digital Ground
J1-172	DGND	--	--	--	GND	Digital Ground
J1-173	DGND	--	--	--	GND	Digital Ground
J1-174	DGND	--	--	--	GND	Digital Ground
J1-175	DGND	--	--	--	GND	Digital Ground
J1-176	DGND	--	--	--	GND	Digital Ground
J1-177	DGND	--	--	--	GND	Digital Ground
J1-178	DGND	--	--	--	GND	Digital Ground
J1-179	DGND	--	--	--	GND	Digital Ground
J1-180	DGND	--	--	--	GND	Digital Ground

Table 27: J1 Baseboard Connector Pin Mappings

TABLE NOTES:

1. **Ethernet voltage levels follow the IEEE 802.3ab specification. Please see the IEEE 802.3ab Specification for more information.**
2. **USB voltage levels follow the USB specification and depend on the USB operating speed. Please see the USB Specification for more information.**
3. **MIPI CSI-2 voltage levels follow the MIPI CSI-2 specification. Please see the MIPI CSI-2 Specification for more information.**
4. **PCIe voltage levels follow the PCIe specification and depend on the operating speed. Please see PCI-SIG for more information.**

11.2 J2 Baseboard Connector

J2 Pin#	Signal Name	BGA Ball#	Processor Alternate Functions	I/O	Voltage (V)	Description
J2-1	FAN_SUPPLY	--	--	PWR	5V/12V	Fan Voltage, 5V/12V option determined by JP61. JP61.1-2 (12V_In), JP61.2-3 (BB_5V_IN).
J2-2	SOM_5V	--	--	PWR	5.0V	Main SOM power input rail.
J2-3	FAN_SUPPLY	--	--	PWR	5V/12V	Fan Voltage, 5V/12V option determined by JP61. JP61.1-2 (12V_In), JP61.2-3 (BB_5V_IN).
J2-4	SOM_5V	--	--	PWR	5.0V	Main SOM power input rail.
J2-5	RSVD_PWM	--	--	O	5V/12V	Fan PWM. Optionally driven by I2C3_SCL. Driver transistor and pull-up not populated by default.
J2-6	SOM_5V	--	--	PWR	5.0V	Main SOM power input rail.
J2-7	FAN_GND	--	--	--	GND	Fan GND
J2-8	SOM_5V	--	--	PWR	5.0V	Main SOM power input rail.
J2-9	FAN_GND	--	--	--	GND	Fan GND
J2-10	SOM_5V	--	--	PWR	5.0V	Main SOM power input rail.
J2-11	VBAK_RTC	--	--	PWR	3.0V	Power rail to the PCF85263ATT RTC on the SOM when SOM_5V is not present.
J2-12	SOM_5V	--	--	PWR	5.0V	Main SOM power input rail.
J2-13	VBAK_GNSS	--	--	PWR	3.0V	Power rail to the Cellular/GNSS on the SOM when SOM_5V is not present.
J2-14	SOM_5V	--	--	PWR	5.0V	Main SOM power input rail.
J2-15	D1.8V_SOM	--	--	PWR	1.8V	D1.8V reference power from the SOM.
J2-16	SOM_5V	--	--	PWR	5.0V	Main SOM power input rail.
J2-17	VDDQVA_SD0	--	--	PWR	1.8/3.3V	SD0 Card IO Voltage
J2-18	SOM_5V	--	--	PWR	5.0V	Main SOM power input rail.
J2-19	VDDQVA_SD1	--	--	PWR	3.3V	SD1 Card IO Voltage. 3.3V by default. Resistor population option on baseboard to change to 1.8V.

J2 Pin#	Signal Name	BGA Ball#	Processor Alternate Functions	I/O	Voltage (V)	Description
J2-20	SOM_5V	--	--	PWR	5.0V	Main SOM power input rail.
J2-21	D3.3V_SOM	--	--	PWR	3.3V	D3.3V reference power from the SOM.
J2-22	SOM_5V	--	--	PWR	5.0V	Main SOM power input rail.
J2-23	D3.3V_SOM	--	--	PWR	3.3V	D3.3V reference power from the SOM.
J2-24	SOM_5V	--	--	PWR	5.0V	Main SOM power input rail.
J2-25	DGND	--	--	--	GND	Digital Ground
J2-26	SOM_5V	--	--	PWR	5.0V	Main SOM power input rail.
J2-27	DDR_1.8V	--	--	--	1.8V	Test only
J2-28	SOM_5V	--	--	PWR	5.0V	Main SOM power input rail.
J2-29	DDR0_1.1V	--	--	--	1.1V	Analog detection of last SOM power supply
J2-30	SOM_5V	--	--	PWR	5.0V	Main SOM power input rail.
J2-31	DDR1_1.1V	--	--	--	1.1V	Test only
J2-32	SOM_5V	--	--	PWR	5.0V	Main SOM power input rail.
J2-33	VDD0.8V	--	--	--	0.8V	Test only
J2-34	SOM_5V	--	--	PWR	5.0V	Main SOM power input rail.
J2-35	DVFS0.8V	--	--	--	0.8V	Test only
J2-36	SOM_5V	--	--	PWR	5.0V	Main SOM power input rail.
J2-37	VDD_CELLULAR	--	--	--	3.3V	Test only
J2-38	SOM_5V	--	--	PWR	5.0V	Main SOM power input rail.
J2-39	VLDO_2.5V	--	--	--	2.5V	Test only
J2-40	SOM_5V	--	--	PWR	5.0V	Main SOM power input rail.
J2-41	PWRGOOD_BB_EN	--	--	I	3.3V	Digital indication of SOM power supplies ready
J2-42	PRESETOUTN	AA5	PRESETOUT#	I	3.3V	Peripheral Reset
J2-43	GP6_30_LDO_VSEL	AJ31	GP6_30/AUDIO_CLKOUT2_B/SSI_SCK9_B/TPU0TO2	I	3.3V	SD0 1.8V/3.3V LDO control
J2-44	PRESETN_18	AL18	PRESET#	O	1.8V	Reset
J2-45	GP6_13_SUPRVSR_ INTn	AF33	GP6_13/SSI_SDATA5	I	3.3V	Power Button

J2 Pin#	Signal Name	BGA Ball#	Processor Alternate Functions	I/O	Voltage (V)	Description
J2-46	SOM_ENABLE	--		O		Enable SOM Power Supplies
J2-47	GP6_11_SUPRVSR_KILLn	AF32	GP6_11/SSI_SCK5	I	3.3V	Kill Signal
J2-48	D1.8V_SOM	--	--	PWR	1.8V	D1.8V reference power from the SOM.
J2-49	DGND	--	--	--	GND	Digital Ground
J2-50	TRSTN_18	AM34	TRST#	O	1.8V	JTAG
J2-51	GP7_3	AL3	GP7_03	I	3.3V	LED control, D9
J2-52	TDI_18	AL34	TDI	O	1.8V	JTAG
J2-53	AVS2/GP7_1	AK3	AVS2/GP7_01	I	3.3V	LED control, D8
J2-54	TDO_18	AL33	TDO	I	1.8V	JTAG
J2-55	AVS1/GP7_0	AJ5	AVS1/GP7_00	I	3.3V	LED control, D7
J2-56	TCK_18	AL32	TCK	I	1.8V	JTAG
J2-57	GP0_4	AH6	MD11/GP0_4/MSIOF2_SCK_B/VI4_DATA20/VI5_DATA4	I	3.3V	LED control, D6
J2-58	TMS_18	AM33	TMS	I/O	1.8V	JTAG
J2-59	GP5_22/SOFTSW2	W33	GP5_22/MSIOF0_RXD	O	3.3V	Switch, “Center”
J2-60	DGND	--	--	--	GND	Digital Ground
J2-61	GP5_20/SOFTSW1	W34	GP5_20/MSIOF0_TXD	O	3.3V	Switch, “Right”
J2-62	GP6_3/SSI_SDATA1_A	AD30	GP6_03/SSI_SDATA1_A	I/O	3.3V	Audio Codec D1
J2-63	GP5_17/SOFTSW0	V35	GP5_17/MSIOF0_SCK	O	3.3V	Switch, “Down”
J2-64	GP6_2/SSI_SDATA0/MSIOF1_SS2_F	AD33	GP6_02/SSI_SDATA0/MSIOF1_SS2_F	I/O	3.3V	Audio Codec D0
J2-65	GP3_13	V30	GP3_13/SD0_WP/NFDATA15_A/SDA2_B	O	3.3V	Switch, “Left”
J2-66	GP6_1/SSI_WS01239/MSIOF1_SS1_F	AC33	GP6_01/SSI_WS01239/MSIOF1_SS1_F	I	3.3V	Audio Codec LRCLK
J2-67	GP4_06	P30	GP4_06/SD2_DS (MMC0_DS)/NFALE	O	3.3V / 1.8V	Switch, “Up”
J2-68	GP6_0/SSI_SCK01239/MSIOF1_TXD_F	AC34	GP6_00/SSI_SCK01239/MSIOF1_TXD_F	I	3.3V	Audio Codec BCLK
J2-69	DGND	--	--	--	GND	Digital Ground
J2-70	DGND	--	--	--	GND	Digital Ground

J2 Pin#	Signal Name	BGA Ball#	Processor Alternate Functions	I/O	Voltage (V)	Description
J2-71	NMI_18	AK31	NMI	--	1.8V	Test Point
J2-72	AUDIO_CLKB	W32	GP5_12/HSCK0/MSIOF1_SCK_D/AUDIO_CLKB_A/SSI_SDATA1_B/RX5_B	O	3.3V	Audio CLK (512x44.1kHz)
J2-73	GP5_18	W35	GP5_18/MSIOF0_SYNC/AUDIO_CLKOUT_A/TX5_B	--	3.3V	Test point
J2-74	AUDIO_CLKA	AD35	GP6_22/ AUDIO_CLKA_A	O	3.3V	Audio CLK (512x48kHz)
J2-75	GP6_7/SSI_SDATA3	AE32	GP6_07/SSI_SDATA3/HRTS2#_A/MSIOF1_TXD_A	I/O	3.3V	External GPIO
J2-76	DGND	--	--	--	GND	Digital Ground
J2-77	GP1_20	AB1	GP1_20/CS0#/VI5_CLKENB	I/O	3.3V	External GPIO
J2-78	SD1_CMD_V	T30	GP3_07/SD1_CMD/MSIOF1_SYNC_G/NFCE#_B	I/O	3.3V / 1.8V	External GPIO
J2-79	GP6_14	AF31	GP6_14/SSI_SCK6	I/O	3.3V	External GPIO
J2-80	SD1_DAT0_V	R33	GP3_08/SD1_DAT0/SD2_DAT4 (MMC0_DAT4)/MSIOF1_RXD_G/NFWP#_B	I/O	3.3V / 1.8V	External GPIO/SPI
J2-81	GP6_15	AF30	GP6_15/SSI_WS6	I/O	3.3V	External GPIO
J2-82	SD1_DAT1_V	R31	GP3_09/SD1_DAT1/SD2_DAT5 (MMC0_DAT5)/MSIOF1_TXD_G/NFDATA14_B	I/O	3.3V / 1.8V	External GPIO/SPI
J2-83	GP6_21	AH35	GP6_21/SSI_SDATA9_A/HSCK2_B/MSIOF1_SS1_C/HSCK1_A/SSI_WS1_B/ SCK1/SCK5_A	I/O	3.3V	External GPIO
J2-84	SD1_DAT2_V	R30	GP3_10/SD1_DAT2/SD2_DAT6 (MMC0_DAT6)/MSIOF1_SS1_G/NFDATA15_B	I/O	3.3V / 1.8V	External GPIO/SPI
J2-85	GP6_31	AJ32	GP6_31/GP6_31/AUDIO_CLKOUT3_B/SSI_WS9_B/TPU0TO3	I/O	3.3V	External GPIO
J2-86	SD1_DAT3_V	T31	GP3_11/SD1_DAT3/SD2_DAT7 (MMC0_DAT7)/MSIOF1_SS2_G/NFRB#_B	I/O	3.3V / 1.8V	External GPIO/SPI
J2-87	GP1_9	AE1	GP1_09/MSIOF2_SCK_A/CTS4#_B/VI5_VSYNC#	I/O	3.3V	External GPIO/SPI
J2-88	DGND	--	--	--	GND	Digital Ground
J2-89	GP0_1	AJ3	MD0/GP0_01/MSIOF2_SS2_B/MSIOF3_SYNC_A/VI4_DATA17/VI5_DATA1	I/O	3.3V	External GPIO/SPI
J2-90	SD1_CLK_V	R35	GP3_06/SD1_CLK/MSIOF1_SCK_G	I/O	3.3V / 1.8V	External GPIO/SPI
J2-91	GP0_0	AJ4	GP0_00/MSIOF2_SS1_B/MSIOF3_SCK_A/VI4_DATA16/VI5_DATA0	I/O	3.3V	External GPIO/SPI
J2-92	DGND	--	--	--	GND	Digital Ground
J2-93	MD20/GP1_10	AD6	MD20/GP1_10/MSIOF2_RXD_A/RTS4#_B/VI5_HSYNC#	I/O	3.3V	External GPIO/SPI
J2-94	SD0_CLK_V	T35	GP3_00/SD0_CLK/MSIOF1_SCK_E	I	3.3V / 1.8V	SD Card Clock

J2 Pin#	Signal Name	BGA Ball#	Processor Alternate Functions	I/O	Voltage (V)	Description
J2-95	GP1_21/DU_ON_ OFF	AA1	GP1_21/CS1#/VI5_CLK/EX_WAIT0_B	I	3.3V	RGB ON/OFF
J2-96	DGND	--	--	--	GND	Digital Ground
J2-97	GP2_1/DU_DE	Y3	GP2_01/IRQ1/DU_DISP/VI4_DATA1_B/CAN0_RX_B/CANFD0_RX_B/ MSIOF3_SS1_E	I	3.3V	RGB Data En
J2-98	SD0_CD	V31	GP3_12/SD0_CD/NFDATA14_A/SCL2_B	O	3.3V	SD0 Card Detect
J2-99	DGND	--	--	--	GND	Digital Ground
J2-100	SD0_CMD_V	U33	GP3_01/SD0_CMD/MSIOF1_SYNC_E	I	3.3V / 1.8V	SD0 CMD
J2-101	DU_VSYNC	Y6	GP2_05/IRQ5/DU_EXVSYNC/DU_VSYNC/VI4_DATA5_B/MSIOF3_TXD_E/PWM6_B	I	3.3V	RGB VSYNC
J2-102	SD0_DAT3_V	U34	GP3_05/SD0_DAT3/MSIOF1_SS2_E	I/O	3.3V / 1.8V	SD0 D3
J2-103	DU_HSYNC	Y5	GP2_04/IRQ4/DU_EXHSYNC/DU_HSYNC/VI4_DATA4_B/MSIOF3_RXD_E/PWM5_B	I	3.3V	RGB HSYNC
J2-104	SD0_DAT2_V	U35	GP3_04/SD0_DAT2/MSIOF1_SS1_E	I/O	3.3V / 1.8V	SD D2
J2-105	DGND	--	--	--	GND	Digital Ground
J2-106	SD0_DAT1_V	T32	GP3_03/SD0_DAT1/MSIOF1_TXD_E	I/O	3.3V / 1.8V	SD D1
J2-107	DU_DB7	AE3	MD22/GP1_07/MSIOF2_SS2_A/TX4_B/VI4_DATA15/VI5_DATA15/DU_DB7	I	3.3V	RGB Blue 7
J2-108	SD0_DAT0_V	T33	GP3_02/SD0_DAT0/MSIOF1_RXD_E	I/O	3.3V / 1.8V	SD D0
J2-109	DU_DB6	AE4	MD23/GP1_06/MSIOF2_SS1_A/RX4_B/VI4_DATA14/VI5_DATA14/DU_DB6	I	3.3V	RGB Blue 6
J2-110	DGND	--	--	--	GND	Digital Ground
J2-111	DU_DB5	AE5	GP1_05/MSIOF3_SS2_B/SCK4_B/VI4_DATA13/VI5_DATA13/DU_DB5	I	3.3V	RGB Blue5
J2-112	GP5_01/RX0/ HRX1_B	Y31	GP5_01/RX0/HRX1_B	O	3.3V	External UART0 RX
J2-113	DU_DB4	AE6	MD25/GP1_04/MSIOF3_SS1_B/VI4_DATA12/VI5_DATA12/DU_DB4	I	3.3V	RGB Blue4
J2-114	GP5_02/TX0/ HTX1_B	Y30	GP5_02/TX0/HTX1_B	I	3.3V	External UART0 TX
J2-115	DU_DB3	AF1	MD26/GP1_03/MSIOF3_RXD_B/VI4_DATA11/DU_DB3/PWM6_A	I	3.3V	RGB Blue 3
J2-116	DGND	--	--	--	GND	Digital Ground
J2-117	DU_DB2	AF2	GP1_02/MSIOF3_SCK_B/VI4_DATA10/DU_DB2/PWM5_A	I	3.3V	RGB Blue 2
J2-118	SCIF2_RXD	AB33	GP5_11/RX2_A/SD2_WP_B/SDA1_A	O	3.3V	Debug serial

J2 Pin#	Signal Name	BGA Ball#	Processor Alternate Functions	I/O	Voltage (V)	Description
J2-119	DU_DB1	AF4	MD27/GP1_01/MSIOF3_TXD_B/VI4_DATA9/DU_DB1/PWM4_A	I	3.3V	RGB Blue 1
J2-120	SCIF2_TXD	AB34	GP5_10/TX2_A/SD2_CD_B/SCL1_A	I	3.3V	Debug serial
J2-121	DU_DB0	AF6	MD28/GP1_00/A0/MSIOF3_SYNC_B/VI4_DATA8/DU_DB0/PWM3_A	I	3.3V	RGB Blue 0
J2-122	HSCIF2_HRX	AF35	GP6_08/SSI_SCK4/HRX2_A/MSIOF1_SCK_A	O	3.3V	Debug serial (secondary)
J2-123	DGND	--	--	--	GND	Digital Ground
J2-124	HSCIF2_HTX	AE30	GP6_09/SSI_WS4/HTX2_A/MSIOF1_SYNC_A	I	3.3V	Debug serial (secondary)
J2-125	DU_DG7	AC6	MD17/GP1_15/MSIOF3_TXD_C/HRTS4#/VI5_DATA11/DU_DG7	I	3.3V	RGB Green 7
J2-126	DGND	--	--	--	GND	Digital Ground
J2-127	DU_DG6	AD2	MD18/GP1_14/MSIOF3_RXD_C/HCTS4#/VI5_DATA10/DU_DG6	I	3.3V	RGB Green 6
J2-128	USB21_DM1	AP32	DM1	I/O	3.3V	USB 2.0 D-
J2-129	DU_DG5	AD3	MD19/GP1_13/MSIOF3_SYNC_C/HTX4_A/VI5_DATA9/DU_DG5	I	3.3V	RGB Green 5
J2-130	USB21_DP1	AR32	DP1	I/O	3.3V	USB 2.0 D+
J2-131	MD21/DU_DG4	AD4	MD21/GP1_12/MSIOF3_SCK_C/HRX4_A/VI5_DATA8/DU_DG4	I	3.3V	Boot Mode / RGB Green 4
J2-132	DGND	--	--	--	GND	Digital Ground
J2-133	DU_DG3	AB4	MD13/GP1_19/VI4_CLKENB/DU_DG3	I	3.3V	RGB Green 3
J2-134	USB1_OVC	AH33	GP6_27/USB1_OVC/MSIOF1_SS2_C/SSI_WS1_A/HCTS2#_C	O	3.3V	USB 2.0 Over Current
J2-135	DU_DG2	AC1	MD14/GP1_18/VI4_HSYNC#/DU_DG2	I	3.3V	RGB Green 2
J2-136	USB1_PWEN	AH34	GP6_26/USB1_PWEN/SSI_SCK1_A/HTX2_C	I	3.3V	USB 2.0 Power EN
J2-137	MD15/DU_DG1	AC2	MD15/GP1_17/VI4_VSYNC#/DU_DG1	I/O	3.3V	Boot Mode / RGB Green 1
J2-138	USB20_VBUS0	AM31	VBUS0	O	-	USB 2.0 VBUS detect
J2-139	DU_DG0	AC4	MD16/GP1_16/VI4_FIELD/DU_DG0	I	3.3V	RGB Green 0
J2-140	USB20_ID0	AN31	ID0	O	3.3V	USB 2.0 ID
J2-141	DGND	--	--	--	GND	Digital Ground
J2-142	USB0_OVC	AH32	GP6_25/USB0_OVC/HRX2_C	O	3.3V	USB 2.0 Overcurrent
J2-143	DU_DR7/MSIOF3_ SS2_A	AG1	GP0_15/MSIOF3_SS2_A/HTX3_C/VI4_DATA7_A/DU_DR7/SDA6_C	I	3.3V	RGB Red 7
J2-144	USB0_PWEN	AH31	GP6_24/USB0_PWEN/HSCK2_C	I	3.3V	USB 2.0 Power EN
J2-145	DU_DR6/MSIOF3_ SS1_A	AG2	GP0_14/MSIOF3_SS1_A/HRX3_C/VI4_DATA6_A/DU_DR6/SCL6_C	I	3.3V	RGB Red 6
J2-146	DGND	--	--	--	GND	Digital Ground
J2-147	DU_DR5	AG3	MD10/GP0_13/MSIOF2_SS2_D/TX4_C/VI4_DATA5_A/DU_DR5	I	3.3V	RGB Red 5

J2 Pin#	Signal Name	BGA Ball#	Processor Alternate Functions	I/O	Voltage (V)	Description
J2-148	USB20_DM0	AR33	DM0	I/O	3.3V	USB 2.0 D-
J2-149	DU_DR4	AG4	MD9/GP0_12/MSIOF2_SS1_D/RX4_C/VI4_DATA4_A/DU_DR4	I	3.3V	RGB Red 4
J2-150	USB20_DP0	AP33	DP0	I/O	3.3V	USB 2.0 D+
J2-151	DU_DR3	AG5	MD8/GP0_11/MSIOF2_TXD_D/HTX3_B/VI4_DATA3_A/RTS4#_C/DU_DR3	I	3.3V	RGB Red 3
J2-152	DGND	--	--	--	GND	Digital Ground
J2-153	DU_DR2	AG6	MD7/GP0_10/MSIOF2_RXD_D/HRX3_B/VI4_DATA2_A/CTS4#_C/DU_DR2	I	3.3V	RGB Red 2
J2-154	GP6_16	AG35	GP6_16/SSI_SDATA6	I/O	3.3V	GPIO
J2-155	MD6/DU_DR1	AH1	MD6/GP0_09/MSIOF2_SYNC_D/VI4_DATA1_A/DU_DR1	I/O	3.3V	Boot Mode / RGB Red 1
J2-156	GP6_5/OTG_STAT1	AE34	GP6_05/SSI_SCK349/MSIOF1_SS1_A	I/O	3.3V	External GPIO
J2-157	DU_DR0	AH2	MD12/GP0_08/MSIOF2_SCK_D/SCK4_C/VI4_DATA0_A/DU_DR0	I	3.3V	RGB Red 0
J2-158	GP6_6/OTG_STAT2	AE33	GP6_06/SSI_WS349/HCTS2#_A/MSIOF1_SS2_A	I/O	3.3V	External GPIO
J2-159	DGND	--	--	--	GND	Digital Ground
J2-160	GP6_10/USB_HUB_RESET	AE31	GP6_10/SSI_SDATA4/HSCK2_A/MSIOF1_RXD_A	I	3.3V	USB Hub Reset
J2-161	DU_CLK	Y1	GP2_03/IRQ3/DU_DOTCLKOUT1/VI4_DATA3_B/MSIOF3_SCK_E/PWM4_B	I	3.3V	RGB Clock
J2-162	--	--	--	--	--	Reserved for future use. Do not connect.
J2-163	DGND	--	--	--	GND	Digital Ground
J2-164	--	--	--	--	--	Reserved for future use. Do not connect.
J2-165	I2C6_SDA	AE2	GP1_08/RX3_B/MSIOF2_SYNC_A/HRX4_B/SDA6_A/AVB_AVTP_MATCH_B/PWM1_B	I/O	3.3V	External GPIO/I2C
J2-166	I2C3_SDA	W1	GP2_08/PWM2_A/HTX3_D/SDA3	I/O	3.3V	External GPIO/I2C
J2-167	I2C6_SCL	AD5	GP1_11/TX3_B/MSIOF2_TXD_A/HTX4_B/HSCK4/VI5_FIELD/SCL6_A/AVB_AVTP_CAPTURE_B/PWM2_B	I	3.3V	External GPIO/I2C
J2-168	I2C3_SCL	W2	GP2_07/PWM1_A/HRX3_D/VI4_DATA7_B/SCL3	I	3.3V	PWM
J2-169	I2C5_SDA	V4	GP2_14/AVB_AVTP_CAPTURE_A/MSIOF2_TXD_C/RTS4#_A/SDA5	I/O	3.3V	Touch Screen I2C
J2-170	I2C2_SDA	Y35	GP5_00/SCK0/HSCK1_B/MSIOF_SS2_B/AUDIO_CLKC_B/SDA2_A/SCK5_B	I/O	3.3V	Camera I2C
J2-171	I2C5_SCL	V5	GP2_13/AVB_AVTP_MATCH_A/MSIOF2_RXD_C/CTS4#_A	I	3.3V	Touch Screen I2C
J2-172	I2C2_SCL	AA34	GP5_04/RTS0#/HRTS1#_B/MSIOF1_SS1_B/AUDIO_CLKA_B/SCL2_A/	I	3.3V	Camera I2C
J2-173	I2C1_SDA	AB32	GP5_24/MLB_SIG/RX1_B/MSIOF1_SYNC_F/SDA1_B	I/O	3.3V	External GPIO/I2C

J2 Pin#	Signal Name	BGA Ball#	Processor Alternate Functions	I/O	Voltage (V)	Description
J2-174	SIM_CLK	--	--	I	1.8/3.0V	SIM Clock
J2-175	I2C1_SCL	AC35	GP5_23/MLB_CLK/MSIOF1_SCK_F/SCL1_B	I	3.3V	External GPIO/I2C
J2-176	SIM_IO	--	--	I/O	1.8/3.0V	SIM Data
J2-177	I2C0_SDA	U31	GP3_15/SD1_WP/NFCE#_A/SDA0	I/O	3.3V	External GPIO/I2C
J2-178	SIM_RST	--	--	I	1.8/3.0V	SIM Reset
J2-179	I2C0_SCL	U32	GP3_14/SD1_CD/NFRB#_A/SCL0	I	3.3V	External GPIO/I2C
J2-180	SIM_VSIM	--	--	PWR	1.8/3.0V	SIM Voltage

TABLE 28: J2 **BASEBOARD CONNECTOR PIN MAPPINGS**

Appendix A: Additional Documentation

Software Documentation[7]

RZ/G2 SOM Series YOCTO Linux User Guide[8]

Hardware Documentation

Beacon's RZ/G2 SOM Product Brief
Beacon's RZ/G2 SOM Hardware Specification

Additional Documentation Resources

NXP's PCF85263ATT Datasheet

[7] May require a Beacon EmbeddedWorks login account and product registration to download Beacon EmbeddedWorks documents.
[8] https://support.logicpd.com/DesktopModules/Bring2mind/DMX/Download.aspx?portalid=0&EntryId=3350