i.MX 8M Plus Development Kit

User Guide

Beacon EmbeddedWorks
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Revision History

REV	EDITOR	DESCRIPTION	SCHEMATIC PN & REV	APPROVAL	DATE
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B	A.Ford	Fix Typo in footer		N.Kro	11/3/2023

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1 Introduction

This user guide continues where the QuickStart Guide ended by providing additional hardware details about the i.MX 8M Plus Development Kit. The purpose of this document is to present information that may be useful after you have unpacked your kit, run through the demo, and are ready to begin development work. This document also points you to other resources depending upon your specific development needs.

1.1 Scope of Document

This user guide does not provide detailed instructions for the software included with the kit. Please refer to the specific user guides for each respective software product for additional information. A list of additional documentation is available in Appendix A: Additional Documentation.

1.2 Requirements

It is assumed that the QuickStart Guide has been read in its entirety. See Appendix A: Additional Documentation for a link to the QuickStart Guide.

The following items will be needed for the procedures described in this document:

- i.MX 8M Plus Development Kit registered on Beacon EmbeddedWorks' website[1]
- Host PC (the procedures in this document were tested using a Windows 10 host PC)
- USB port
- microSD card reader (included in development kit)
- microSD card (included in development kit)
- Serial cable (USB Type-A standard male to USB Type-B micro male - included in development kit)
- Wattson cable (USB Type-A standard male to USB Type-B mini male - included in development kit)
- Active Internet connection
- Ethernet Cable (included in development kit)
- MOLEX 1461531100 WIFI/Bluetooth Antenna x2
- Terminal emulation program (e.g., Tera Term as described in Section 2.2)

[1] http://support.beaconembedded.com/auth/register_product.php

1.3 i.MX 8M Plus Baseboard Features Diagram

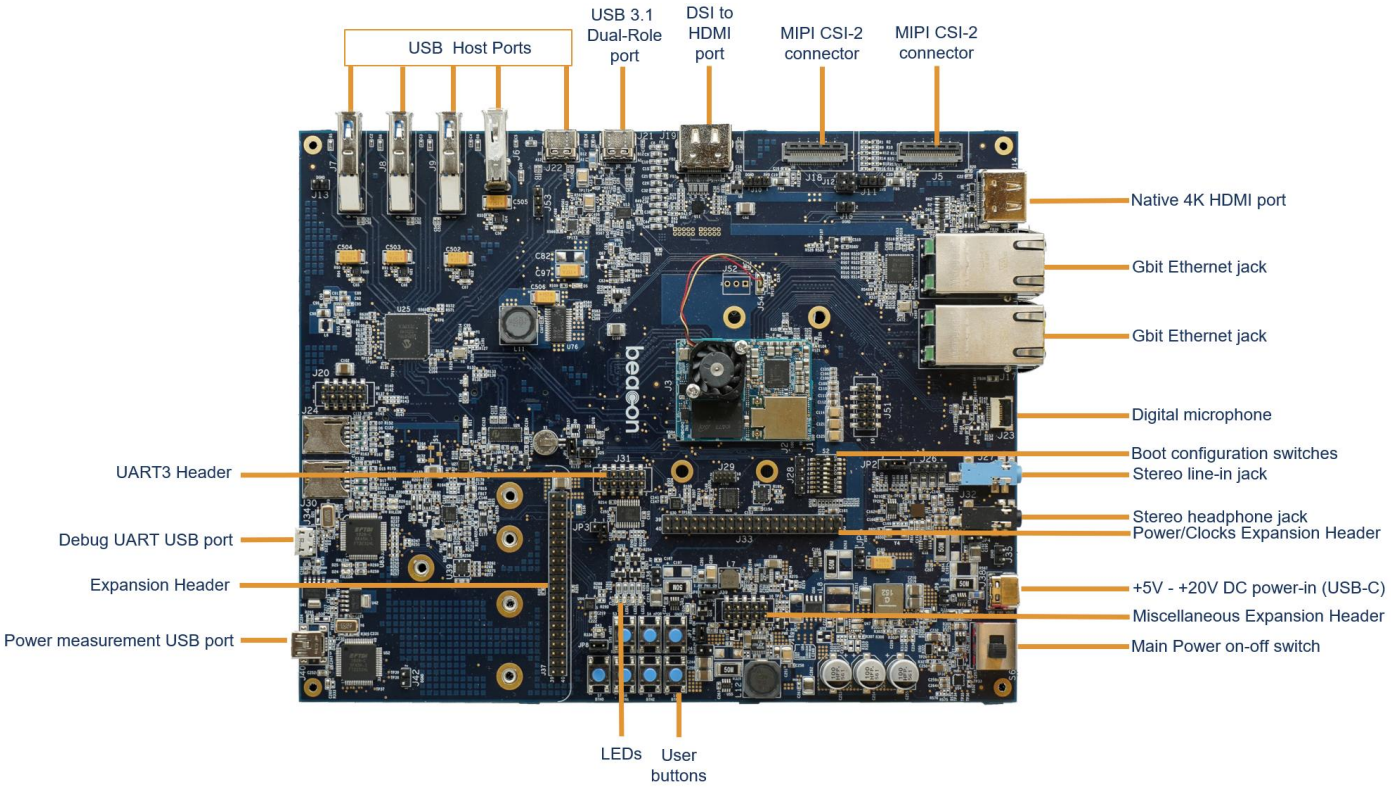

Figure 1: Baseboard (Front Side)

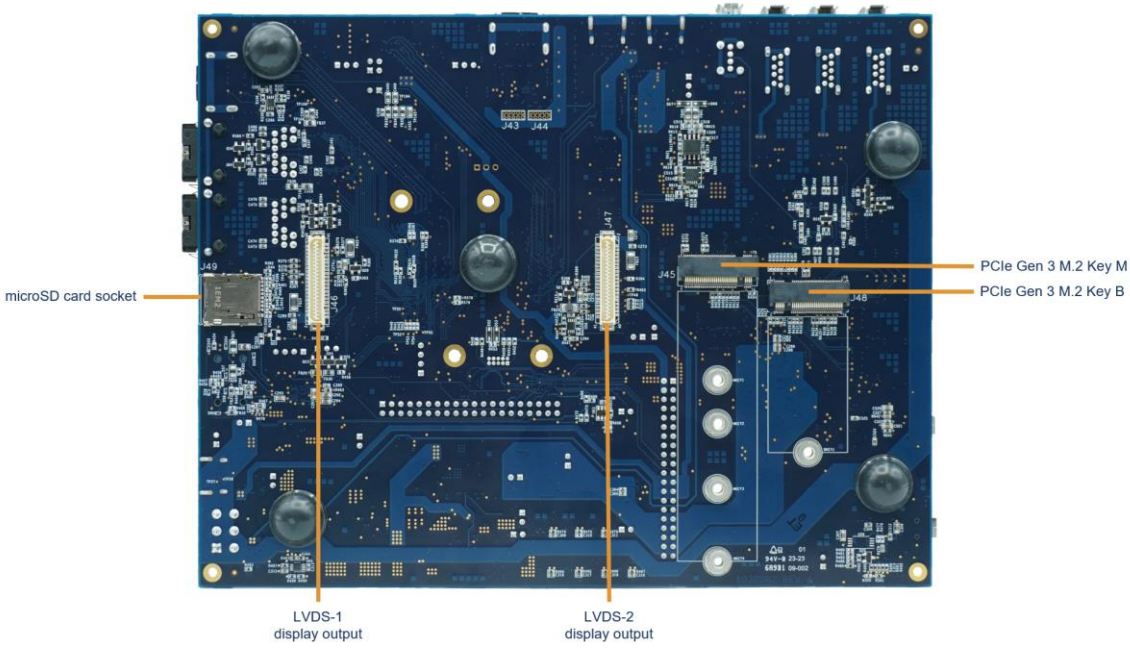

Figure 2: Baseboard (Back Side)

2 Connect Development Kit to PC

To begin development work, the development kit needs to be connected to a host PC.

Follow the steps below to connect the development kit.

1. Connect the USB micro-B cable to the debug UART USB port (J34) on the baseboard and to an empty USB port on your host PC. See Figure 3.

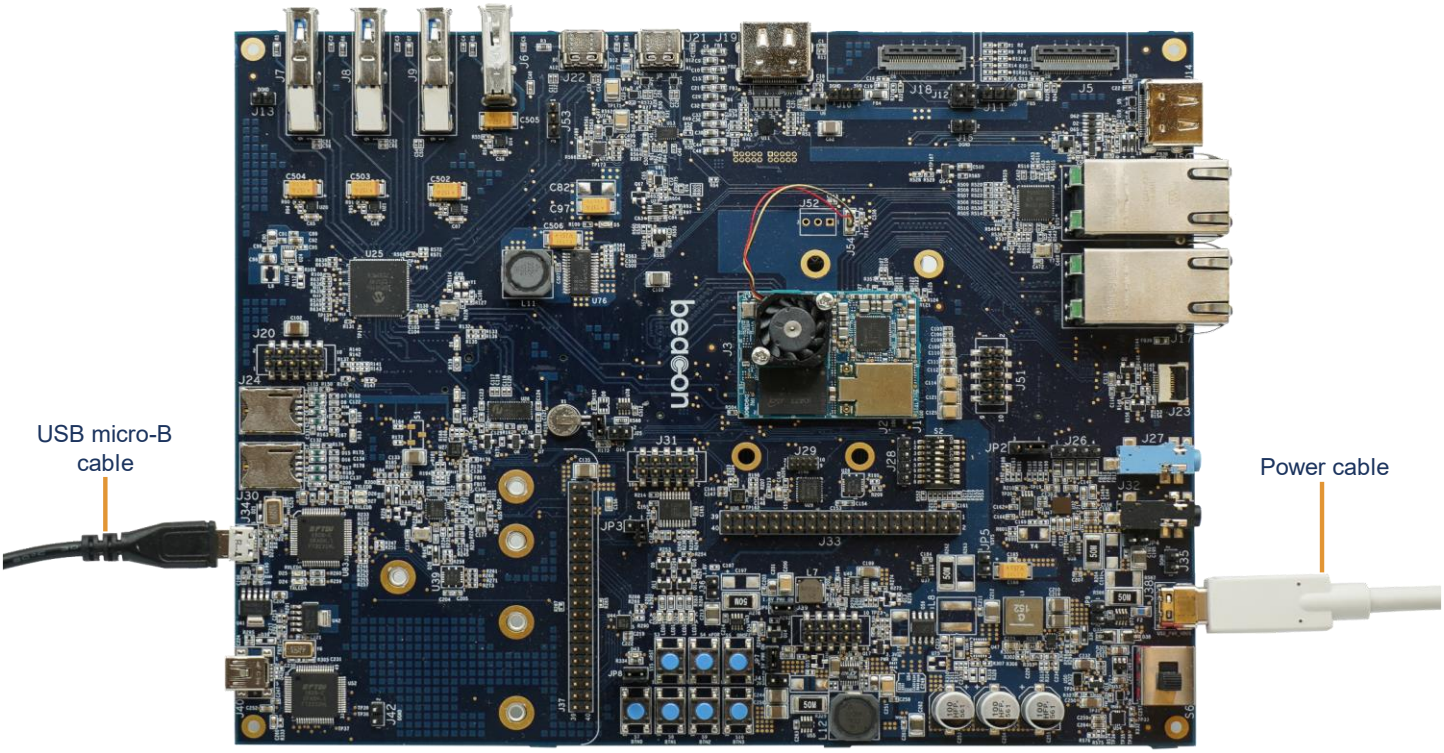

Figure 3: Baseboard (Front Side) w/ Cables

NOTE: The baseboard is equipped with an FTDI virtual COM port (VCP) chip that causes the USB device to appear to your computer as an additional COM port. Settings for the terminal emulation program will remain the same; however, a driver must be installed on your computer for proper operation. A link to the driver and instructions for using the USB-to-UART VCP chip can be found in Beacon EmbeddedWorks' USB-to-UART VCP Chip Driver ReadMe[2]. See section 9.9.1 for more information on how to configure your debug terminal.

2. Plug the power adapter into an electrical outlet and the USB-C cable from the output connector into the power-in connector on the baseboard. See Figure 3.
3. Before powering on your kit, you will have to install a terminal emulation program to communicate with the development kit. Please proceed to the next section for details.

[2] http://support.beaconembedded.com/downloads/910/

3 Install Terminal Emulator Program

The i.MX 8M Plus Development Kit is designed to communicate with terminal emulation programs using the included microUSB cable. Although Beacon EmbeddedWorks does not support any terminal emulation program, we provide steps below for using Tera Term for Windows and minicom for Linux using Ubuntu.

3.1 Setup Windows Serial Terminal

Tera Term can be downloaded for free from Beacon EmbeddedWorks' website. To install Tera Term:

1. Download the ZIP file[3] from Beacon EmbeddedWorks' website and extract the contents.
2. After extracting the contents, locate the teraterm-x.xx.exe file and double-click it.
3. Follow the on-screen instructions to install Tera Term.
    a. Baud rate: **115200**
    b. Data: **8 bits**
    c. Parity: **None**
    d. Stop: **1 bit**
    e. Flow control: **None**

NOTE: The communication port assigned to the development kit is usually the lowest (1st) port associated with the USB cable.

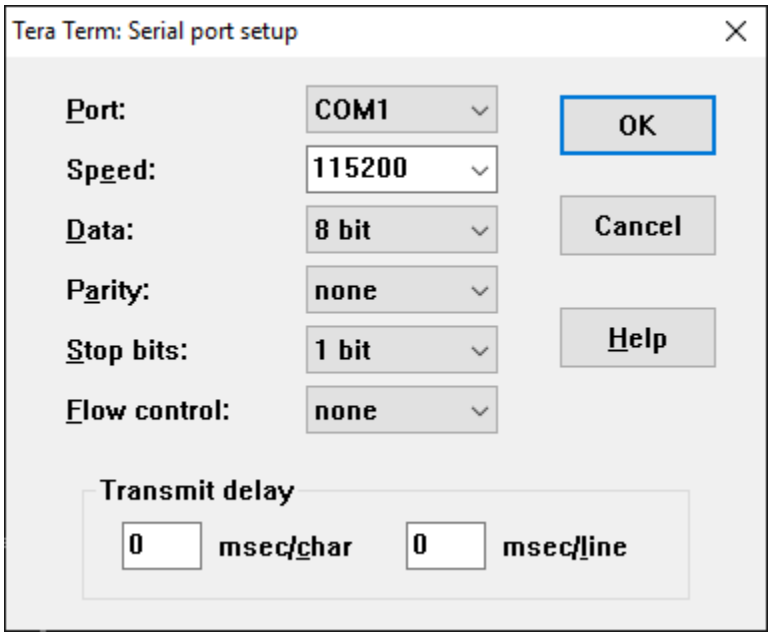

Figure 4: Tera Term Serial Port Settings

4. Click 'OK.'
5. Tera Term serial terminal has been completed.

[3] http://support.beaconembedded.com/downloads/240/

3.2 Setup Linux Serial Terminal

Follow the directions below for installing minicom within Ubuntu.

1. To install minicom, run ‘sudo apt install minicom.’
2. To setup minicom, type ‘sudo minicom -s’
3. Select ‘Serial port setup’

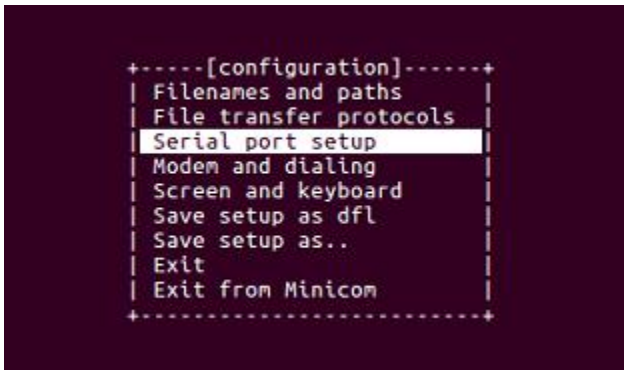

Figure 5: Minicom Configuration Menu

4. Setup the serial port interface specific to the Linux Host PC. This example uses ‘/dev/ttyUSB0’ and the baud rate of 115200 8N1.

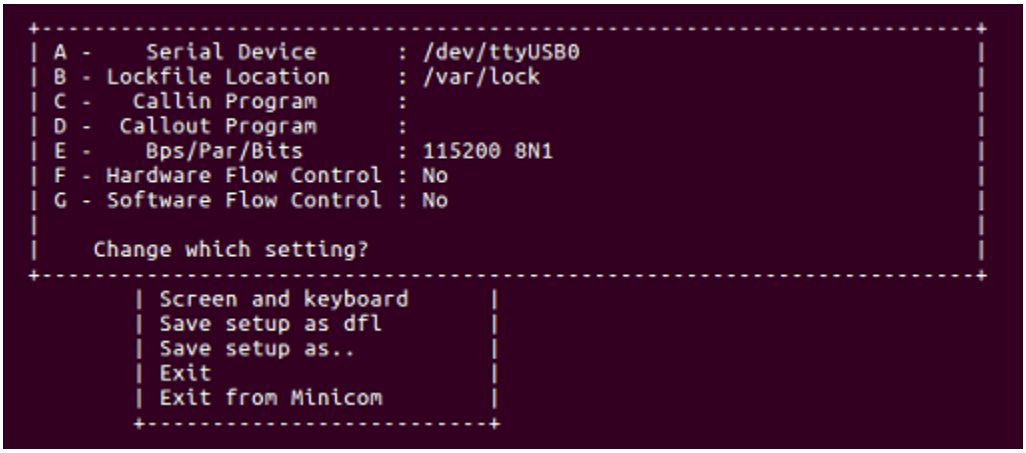

Figure 6: Minicom Serial Port Setup

5. Save setup

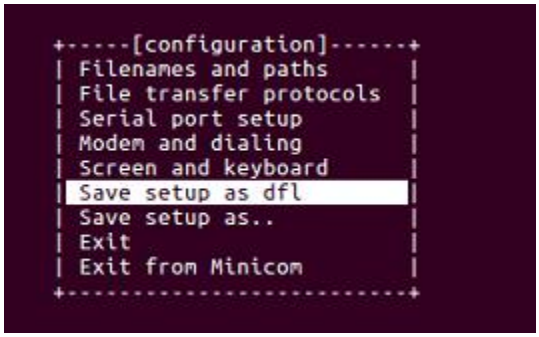

Figure 7: Minicom Save Setup as Default Option

6. Select Exit
7. Minicom serial terminal setup has been completed

4 Boot into U-Boot

U-Boot is a bootloader configured by Beacon EmbeddedWorks to provide the capability for loading the operating system (OS) and applications. In addition, it provides a full suite of commands for interfacing to the System on Module (SOM). These commands load the OS, configure hardware platforms, bring up hardware, customize applications, perform tests, and manage in-field devices.

1. Make sure the development kit is set up as described in Section 2.
2. Remove the pre-built OS image SD card from the baseboard if one is inserted. This step is important because U-Boot boots from onboard flash memory.
3. Verify the boot switches (S2 on the baseboard) are configured to boot from on-board eMMC. See section 10.1 for boot options.

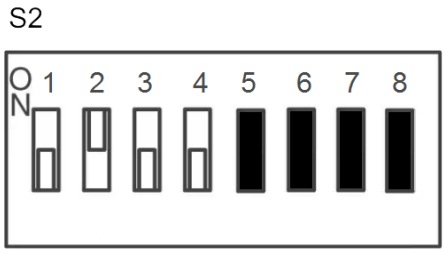

Figure 8: eMMC (SDHC3) Switch Settings

4. Start the terminal emulation program on your host PC.
5. Verify that the serial port settings are correct (see Figure 4 in the previous section).
6. Move the power switch (S6) to the ON position to boot the development kit.
7. Press a key to halt the system at the U-Boot prompt.
8. In your host PC's terminal emulation program, you should see a U-Boot screen like the one below (version numbers and other details may differ from what is shown).

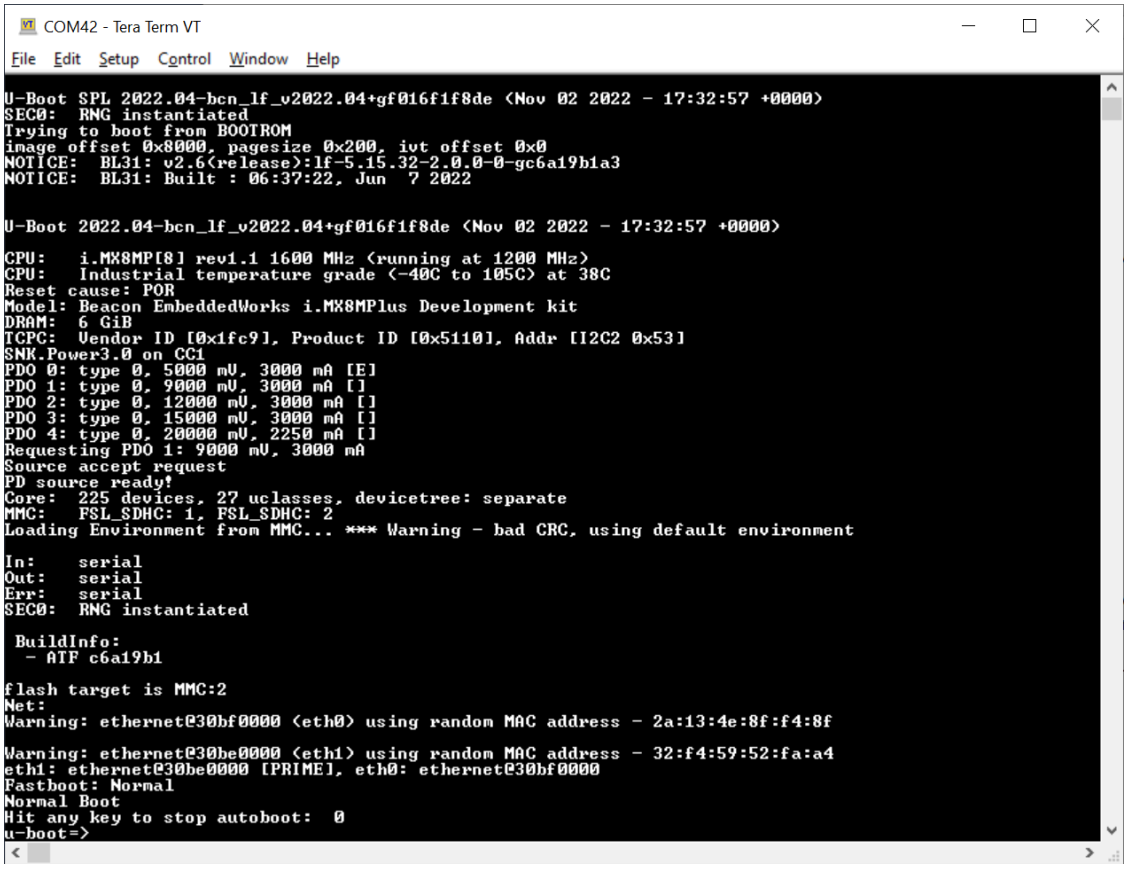

Figure 9: U-Boot Prompt

9. The system is now ready to work with the i.MX 8M Plus SOM using U-Boot. For more information on U-Boot and its capabilities, please see the i.MX 8M Plus SOM Linux Software Developer's Guide provided by Beacon EmbeddedWorks. This document is available on Beacon EmbeddedWorks' support site.

5 Wattson

Wattson is a power measurement and performance monitoring application now standard on all Beacon EmbeddedWorks Development Kits.

The application delivers real-time graphical feedback and data-logging capabilities without the need for external oscilloscopes and meters. Wattson guides you to the lowest power and highest performance software combination for your product.

Wattson is instrumental in helping you minimize power in run, idle, standby, suspend, and system-off states, maximizing battery life in the end application. Wattson is independent of the system, allowing power measurement even when the SOM is in deep-sleep states like suspend and even off.

Wattson runs on Windows and Linux PCs, enabling software development on Linux, Android and Windows IOT-based products.

5.1 How to Get Wattson

Follow the steps below to download and install Wattson.

1. Wattson is available for download from Beacon EmbeddedWorks' website. The links below will launch the download for your specific OS.
   - Wattson for Windows Installer[4] (ZIP file)
   - Wattson for Linux Installer[5] (tar.gz file)

2. Extract the ZIP or tar.gz file. In Linux, the following command will extract the tar.gz:

```
$ tar -xvf wattson_linux.tar.gz
```

In that folder, you will find a *HOW TO INSTALL* document containing installation instructions.

3. Once Wattson is installed on your host PC, a Wattson User Guide is available from the Start > Beacon EmbeddedWorks > Wattson User Guide menu or within the Wattson application under the *Help* menu.

[4] https://support.beaconembedded.com/DesktopModules/Bring2mind/DMX/Download.aspx?portalid=0&EntryId=1416
[5] https://support.beaconembedded.com/DesktopModules/Bring2mind/DMX/Download.aspx?portalid=0&EntryId=1418

5.2 Connect the Development Kit for Wattson

For Wattson to interact with the i.MX 8M Plus Development Kit, use the included USB A to USB mini-B cable to connect the power measurement USB port on the baseboard to an available USB port on your host PC. See Figure 10.

It is recommended to first launch Wattson and connect the USB mini-B cable before connecting the debug UART cable. This will prevent any issues where Wattson might detect the wrong serial debug interface.

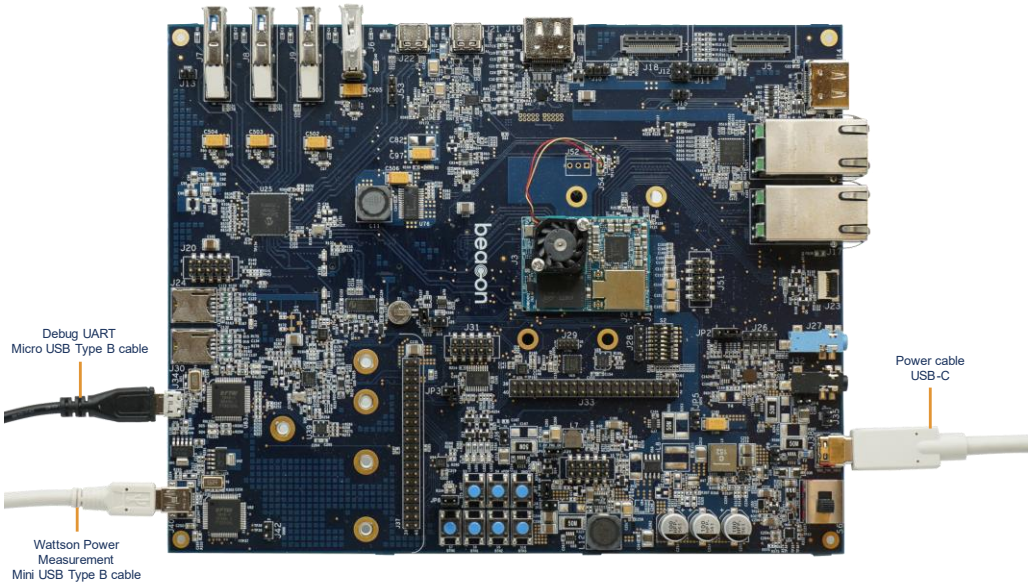

Figure 10: Connect USB mini-B Cable for Wattson

6 Baseboard Jumper Descriptions

The baseboard jumpers as set by default as described in Table 1 and showing in Figure 11.

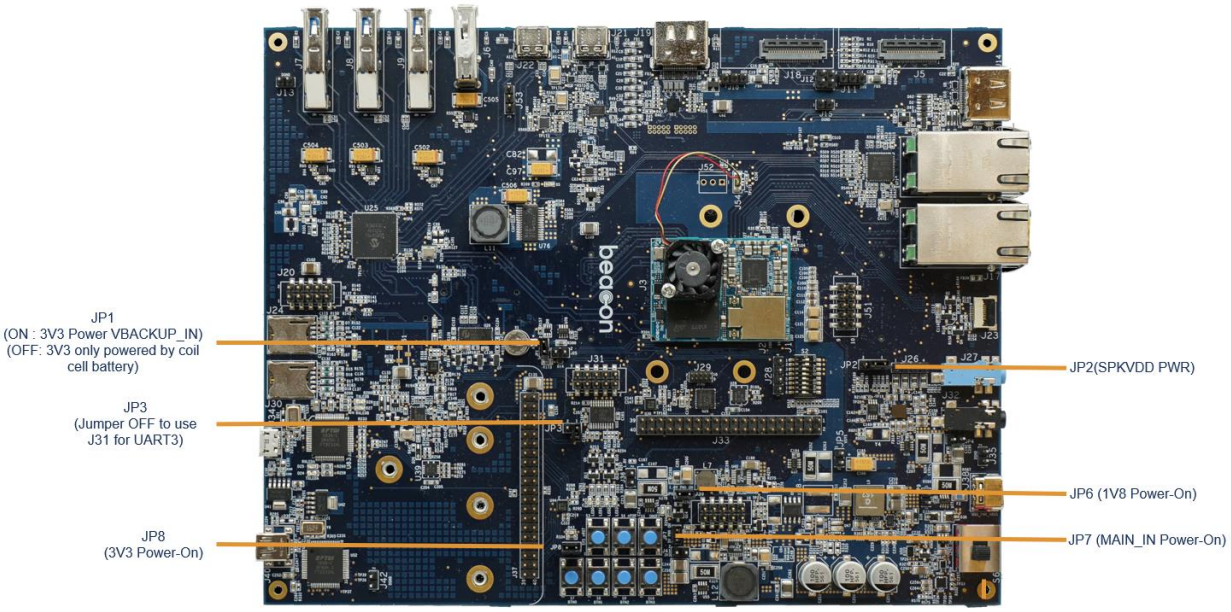

Figure 11: Jumper Locations

Reference Designator	Default Jumper Location	Description
JP1	Across pins 1-2	Used to allow 3V3 to charge the X1 coin cell battery.
JP2	Across pins 1-2	Jumper header made available for the audio CODEC for applications where additional power is required to power the SPKVDD supply. Remove JP2 jumper and apply 5V external supply to JP2.2.
JP3	OFF	Jumper JP3 can be used to turn UART transceiver off to use UART3 on J37.
JP6	Across pins 1-2	Used to allow 1V8 Power-ON LED to function. Allowing the ability to eliminate power on LED for low power applications development.
JP7	Across pins 1-2	Used to allow 5V Power-ON LED to function. Allowing the ability to eliminate power on LED for low power applications development.
JP8	Across pins 1-2	Used to allow 3V3 Power-ON LED to function. Allowing the ability to eliminate power on LED for low power applications development.

Table 1: Available Jumpers

7 Connect Antenna to the i.MX 8M Plus SOM

The i.MX 8M Plus SOM provides two I-Pex MHF4 connector receptacles for connecting 50-ohm dual-band antennas for WiFi and Bluetooth wireless connectivity.

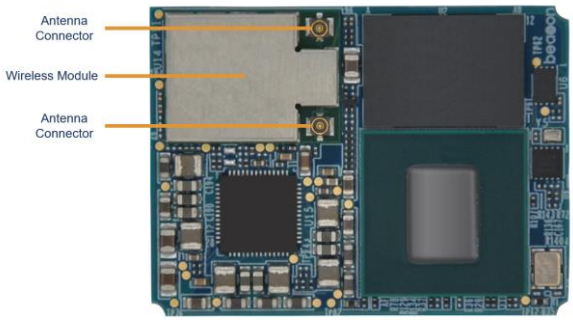

Figure 12: i.MX 8M Plus SOM (Front Side)

IMPORTANT NOTE: The antenna connector on the i.MX 8M Plus SOM is very fragile. Take extreme care when connecting and disconnecting the antenna. If antenna movement is likely in an end-product design, Beacon EmbeddedWorks suggests designing in supports or reinforcements for the antenna and cable on the baseboard to prevent damage to the connector.

7.1 Flat Patch RF Antenna

The Molex 1461531100 is approved for use with the i.MX 8M Plus SOM. The antenna is a 4.5-dBi 50-ohm patch antenna attached to 100 mm miniature coaxial cable with a MHF4 connector at the far end. The antenna supports dual bands: 2.4 GHz and 5.5 GHz.

Figure 13: Molex 2.4GHZ/5.5GHZ Patch Antenna and Integrated Cable

The back of the antenna surface has adhesive to help secure the antenna at the desired location.

8 Powering Down and Waking Up the Development Kit

8.1 Linux

To power down the development kit when using the Linux OS use the *poweroff* command or press the S5 (ON/OFF) button on the baseboard for 5 seconds. Afterwards to power the system back on, press S5 (ON/OFF) button on the baseboard for one second.

The development kit can enter suspend mode from the command line using the command below:

```
root# echo mem > /sys/power/state
```

To wake the development kit from suspend mode, press S5 button.

User can also wake from suspend using the terminal if *no_console_suspend* argument is passed to Linux.

```
u-boot=> setenv optargs no_console_suspend
```

9 Functional Specifications

The block diagram for the i.MX 8M Plus Development Kit is shown below.

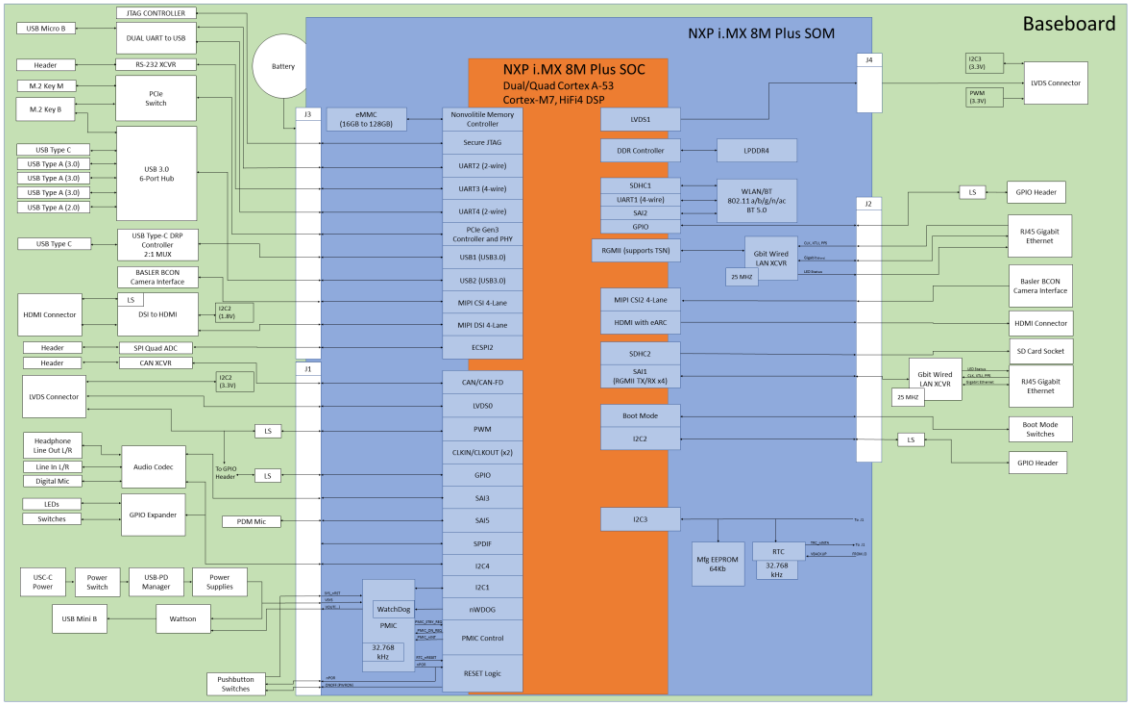

Figure 14: i.MX 8M Plus Dev Kit Block Diagram

9.1 SOM to Baseboard Interface

The baseboard includes three Hirose DF40C-100DS-0.4V(51) 100-pin, double row, 0.4 mm pitch SMT receptacle connectors at locations J1, J2 and J3 for hosting the SOM. All power, grounds, and digital signals traverse through these three host connectors. There is one optional Hirose DF40C-20DS-0.4V(51) 20-pin, double row, 0.4mm pitch connector at location J4 for additional LVDS support.

For the detailed pin mapping of the SOM to baseboard connectors, please refer to section 13 Baseboard Connectors - Pin Descriptions & Functions.

9.2 Clocks

9.2.1 SOM Clocks

9.2.1.1 Processor Clocking

The i.MX 8M Plus processor requires two reference clocks: one for system and high-speed functions and another for low-frequency functions. The high-speed clock connects directly to the processor and the low-speed clock is connected indirectly through the RTC.

Parameter	Min	Typical	Max	Unit
High-speed Processor Crystal (Y1)	--	24.000	--	MHz
Low-speed Crystal (via RTC – Y5)	--	32.768	--	kHz

***Table 2:** Processor Clocks*

9.2.2 Other On-board SOM Clocks

There is also a crystal oscillator on the SOM for the Ethernet transceiver, as enumerated below.

Parameter	Min	Typical	Max	Unit
Ethernet Transceiver Crystal (Y4)	--	25.000	--	MHz

***Table 3: Other On-board SOM** Clocks*

9.2.3 Baseboard Clocks

The baseboard also includes clocks for various functions as listed below.

Parameter	Min	Typical	Max	Unit
Debug FTDI USB to UART Crystal (Y3)	--	6.000	--	MHz
PCIe Clock Crystal (Y5)	--	25.000	--	MHz
Wattson FTDI USB to UART Crystal (Y6)	--	12.000	--	MHz
Ethernet Transceiver Crystal (Y7)	--	25.000	--	MHz
USB Hub Oscillator (Y8)	--	25.000	--	MHz

Table 4: Baseboard Clocks

9.3 Embedded Memory

9.3.1 SOM Memory

The SOM has LPDDR4, eMMC, QSPI NOR flash and a serial EEPROM. See the i.MX 8M Plus Hardware specification for more details on these memories.

9.3.2 Baseboard Memory

The baseboard provides a microSD Card socket at location J49 on the back of the baseboard (see Figure 2 for a picture which includes the uSD card socket).

The processor for i.MX 8M Plus SOM supports up to three Ultra Secure Device Host Controllers (uSDHC) capable of the standard SDIO and SDXC protocol. The SOM reserves uSDHC2 for use on the baseboard using a 4-bit data interface for SD Cards.

In addition, the i.MX 8M Plus processors allow designers to select the voltage levels at which the uSDHC2 interface operates. The SDHC specification requires +3.3V operation by default and can later negotiate +1.8V signaling if supported by the target. The i.MX 8M Plus SOM wires in GPIO1_IO04 as SD2_VSEL which allows the BSP to switch the interface voltage (NVCC_SD2). NVCC_SD2 is driven to 1.8V when SD2_VSEL is high and 3.3V when SD2_VSEL is low.

uSDHC2 operates at 400 kHz (low-speed), 25MHz (normal-speed mode), 50MHz (high-speed mode) or 200MHz (ultra high-speed). The uSDHC2 can operate at either +3.3V or +1.8V on NVCC_SD2 depending on the operating mode.

9.4 Display Interfaces

The i.MX 8M Plus SOM provides a four-lane MIPI display serial interface (DSI), HDMI interface, and two 4-lane LVDS interfaces which are routed directly out to the SOM interface connectors. The i.MX 8M Plus Development Kit converts the MIPI DSI into an HDMI interface.

9.4.1 DSI to HDMI Display

The baseboard converts MIPI DSI to HDMI using an Analog Devices ADV7535 MIPI/DSI Receiver with HDMI Transmitter. The DSI receiver input supports DSI video mode operation only, and specifically, only supports non-burst mode with sync pulses. The DSI receiver provides up to four lanes of MIPI/DSI data, each running up to 891 Mbps. The HDMI transmitter supports video resolutions up to a maximum TMDS clock frequency of 148.5 MHz. The ADV7535 also provides an audio input port, which supports the insertion of audio into the HDMI stream output.

The HDMI signals are connected to a 19-pin HDMI receptacle connector that carries the HDMI display interface, I2C control lines, power, and ground to an external HDMI display.

The HDMI receptacle (Samtec HDMI-19-01-F-SM) is located at J19. See Figure ***1*** which includes the HDMI port at the top, center, of the picture. This 19-pin HDMI high-speed receptacle meets digital display working group single monitor interface specifications.

The pin mapping for the 19-pin HDMI receptacle is shown in the table below. The receptacle also includes four through-hole ground tails for grounding the connector shell.

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain
1	HDMI1_D2_P	HDMI Data 2+	O	1.8V	AVDD_1V8
2	DGND	Digital Ground	PWR	GND	--
3	HDMI1_D2_N	HDMI Data 2-	O	1.8V	AVDD_1V8
4	HDMI1_D1_P	HDMI Data 1+	O	1.8V	AVDD_1V8
5	DGND	Digital Ground	PWR	GND	--
6	HDMI1_D1_N	HDMI Data 1-	O	1.8V	AVDD_1V8
7	HDMI1_D0_P	HDMI Data 0+	O	1.8V	AVDD_1V8
8	DGND	Digital Ground	PWR	GND	--
9	HDMI1_D0_N	HDMI Data 0-	O	1.8V	AVDD_1V8
10	HDMI1_CLK_P	HDMI Clock+	O	1.8V	AVDD_1V8
11	DGND	Digital Ground	PWR	GND	--
12	HDMI1_CLK_N	HDMI Clock-	O	1.8V	AVDD_1V8
13	RFU	--	--	--	--
14	RFU	--	--	--	--
15	HDMI_SCL_CN	DDC_CLK_OUT	O	5.0V	5V0_HDMI
16	HDMI_SDA_CN	DDC_DAT_OUT	I/O	5.0V	5V0_HDMI
17	DGND	Digital Ground	PWR	GND	--
18	5V0_HDMI	+5V Power	PWR	5.0V	5V0
19	HDMI1_HPD	HOTPLUG_DET_OUT	I	5.0V	5V0_HDMI

Table 5: HDMI Receptacle (J19) Pin Mapping

9.4.2 HDMI

The baseboard brings the SOM HDMI signals to a 19-pin HDMI receptacle connector that carries the HDMI display interface, eARC, I2C control lines, power, and ground to an external HDMI display.

The HDMI receptacle (Samtec HDMI-19-01-F-SM) is located at J14. See Figure 1 which includes the HDMI port at the right, top, of the picture. This 19-pin HDMI high-speed receptacle meets digital display working group single monitor interface specifications.

The pin mapping for the 19-pin HDMI receptacle is shown in the table below. The receptacle also includes four through-hole ground tails for grounding the connector shell.

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain
1	HDMI_D2_P	HDMI Data 2+	O	1.8V	AVDD_1V8
2	DGND	Digital Ground	PWR	GND	--
3	HDMI_D2_N	HDMI Data 2-	O	1.8V	AVDD_1V8
4	HDMI_D1_P	HDMI Data 1+	O	1.8V	AVDD_1V8
5	DGND	Digital Ground	PWR	GND	--
6	HDMI_D1_N	HDMI Data 1-	O	1.8V	AVDD_1V8
7	HDMI_D0_P	HDMI Data 0+	O	1.8V	AVDD_1V8
8	DGND	Digital Ground	PWR	GND	--
9	HDMI_D0_N	HDMI Data 0-	O	1.8V	AVDD_1V8
10	HDMI_CLK_P	HDMI Clock+	O	1.8V	AVDD_1V8
11	DGND	Digital Ground	PWR	GND	--
12	HDMI_CLK_N	HDMI Clock-	O	1.8V	AVDD_1V8
13	HDMI_CEC	HDMI Consumer Electronics Control	I/O	1.8V	AVDD_1V8
14	HDMI_UTILITY	EARC P/HDMI Utility	I	1.8V	AVDD_1V8
15	DDC_SCL	DDC_CLK_OUT	O	5.0V	5V0_HDMI
16	DDC_SDA	DDC_DAT_OUT	I/O	5.0V	5V0_HDMI
17	DGND	Digital Ground	PWR	GND	--
18	5V0_HDMI	+5V Power	PWR	5.0V	5V0
19	HDMI_HPD	EARC N/HOTPLUG_DET_OUT	I	5.0V	5V0_HDMI

Table 6: HDMI Receptacle (J14) Pin Mapping

9.4.3 LVDS

The LVDS signals are each connected to a 41-pin display header connector that carries the LVDS display interface, capacitive touch I2C, control lines, power, and backlight PWM control to an external display board.

The LVDS display header connectors (Hirose DF9-41P-1V(32)) are located at J46 and J47 on the back of the baseboard. See Figure 2 for a picture which includes the LVDS display output on the bottom of the baseboard. This 41-pin board-to-board header complies with the standard connector specification for the flat panel display interfaces, VESA FPDI-1 Standard Interface Connector.

The pin mapping for the 41-pin LVDS display header connector is shown in the table below.

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain
1	3V3	3.3V Logic power supply	PWR	3.3V	3V3_IN
2	3V3	3.3V Logic power supply	PWR	3.3V	3V3_IN
3	GND	Ground	PWR	GND	--
4	GND	Ground	PWR	GND	--
5	LVDS0_TX0_P	LVDS differential pair	O	1.8V	1V8
6	LVDS0_TX0_N	LVDS differential pair	O	1.8V	1V8
7	GND	Ground	PWR	GND	--
8	LVDS0_TX1_P	LVDS differential pair	O	1.8V	1V8
9	LVDS0_TX1_N	LVDS differential pair	O	1.8V	1V8
10	GND	Ground	PWR	GND	--
11	LVDS0_TX2_P	LVDS differential pair	O	1.8V	1V8
12	LVDS0_TX2_N	LVDS differential pair	O	1.8V	1V8
13	GND	Ground	PWR	GND	--
14	LVDS0_TX3_P	LVDS differential pair	O	1.8V	1V8
15	LVDS0_TX3_N	LVDS differential pair	O	1.8V	1V8
16	GND	Ground	PWR	GND	--
17	LVDS0_CLK_P	LVDS differential clock	O	1.8V	1V8
18	LVDS0_CLK_N	LVDS differential clock	O	1.8V	1V8
19	GND	Ground	PWR	GND	--
20	GPIO1_IO01	GPIO assigned for PWM to backlight (LCD_PWM0)	O	1.8V	NVCC_GPIO1
21	LCD_RESET	Level-shifted GPIO assigned for LCD reset (GPIO1_IO15)	O	3.3V	3V3
22	LCD_PANEL_PWR	Level-shifted GPIO assigned for enabling LCD power (GPIO1_IO08)	O	3.3V	3V3
23	LVDS0_TCH_nINT	Level-shifted GPIO assigned for interrupt from touch (LVDS0_TCH_INT/GPIO Expander U27, P1_1)	I	3.3V	3V3
24	GND	Ground	PWR	GND	--
25	I2C2_SCL_3V3	Level-shifted I2C clock signal to cap touch	O	3.3V	3V3
26	I2C2_SDA_3V3	Level-shifted I2C data signal to/from cap touch	I/O	3.3V	3V3
27	GND	Ground	PWR	GND	--
28	Reserved	Reserved for test point	--	--	--
29	GND	Ground	PWR	GND	--
30	5V0_LVDS0	5V Backlight power supply	PWR	5.0V	5V0
31	5V0_LVDS0	5V Backlight power supply	PWR	5.0V	5V0
32	5V0_LVDS0	5V Backlight power supply	PWR	5.0V	5V0
33	5V0_LVDS0	5V Backlight power supply	PWR	5.0V	5V0
34	GPIO_EXP_3V3_P1_3	Level-shifted GPIO assigned LCD select	I/O	3.3V	3V3
35	GPIO_EXP_3V3_P1_4	Level-shifted GPIO assigned backlight enable	I/O	3.3V	3V3
36	GPIO_EXP_3V3_P1_5	Level-shifted GPIO assigned touch shutdown	I/O	3.3V	3V3
37	GPIO_EXP_3V3_P1_6	Level-shifted GPIO assigned horizontal polarity	I/O	3.3V	3V3
38	GPIO_EXP_3V3_P1_7	Level-shifted GPIO assigned vertical polarity	I/O	3.3V	3V3
39	GND	Ground	PWR	GND	--
40	GND	Ground	PWR	GND	--
41	GND	Ground	PWR	GND	--

Table 7: LVDS Connector (J46) Pin Mapping

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain
1	3V3	3.3V Logic power supply	PWR	3.3V	3V3_IN
2	3V3	3.3V Logic power supply	PWR	3.3V	3V3_IN
3	GND	Ground	PWR	GND	--
4	GND	Ground	PWR	GND	--
5	LVDS1_TX0_P	LVDS differential pair	O	1.8V	1V8
6	LVDS1_TX0_N	LVDS differential pair	O	1.8V	1V8
7	GND	Ground	PWR	GND	--
8	LVDS1_TX1_P	LVDS differential pair	O	1.8V	1V8
9	LVDS1_TX1_N	LVDS differential pair	O	1.8V	1V8
10	GND	Ground	PWR	GND	--
11	LVDS1_TX2_P	LVDS differential pair	O	1.8V	1V8
12	LVDS1_TX2_N	LVDS differential pair	O	1.8V	1V8
13	GND	Ground	PWR	GND	--
14	LVDS1_TX3_P	LVDS differential pair	O	1.8V	1V8
15	LVDS1_TX3_N	LVDS differential pair	O	1.8V	1V8
16	GND	Ground	PWR	GND	--
17	LVDS1_CLK_P	LVDS differential clock	O	1.8V	1V8
18	LVDS1_CLK_N	LVDS differential clock	O	1.8V	1V8
19	GND	Ground	PWR	GND	--
20	GPIO1_IO09	GPIO assigned for PWM to backlight (LCD_PWM1)	O	1.8V	NVCC_GPIO1
21	GPIO2_EXP_3V3_P1_5 (LCD_RESET1)	Level-shifted GPIO assigned for LCD reset (GPIO2_EXP_3V3_P1_5)	O	3.3V	3V3
22	GPIO2_EXP_3V3_P1_6 (LCD_PANEL_PWR1)	Level-shifted GPIO assigned for enabling LCD power (GPIO2_EXP_3V3_P1_6)	O	3.3V	3V3
23	LVDS1_TCH_nINT	Level-shifted GPIO assigned for interrupt from touch (LVDS1_TCH_INT/GPIO Expander U27, P1_2)	I	3.3V	3V3
24	GND	Ground	PWR	GND	--
25	I2C4_SCL_3V3	Level-shifted I2C clock signal to cap touch	O	3.3V	3V3
26	I2C4_SDA_3V3	Level-shifted I2C data signal to/from cap touch	I/O	3.3V	3V3
27	GND	Ground	PWR	GND	--
28	Reserved	Reserved for test point	--	--	--
29	GND	Ground	PWR	GND	--
30	5V0_LVDS1	5V Backlight power supply	PWR	5.0V	5V0
31	5V0_LVDS1	5V Backlight power supply	PWR	5.0V	5V0
32	5V0_LVDS1	5V Backlight power supply	PWR	5.0V	5V0
33	5V0_LVDS1	5V Backlight power supply	PWR	5.0V	5V0
34	GPIO_EXP_3V3_P0_3	Level-shifted GPIO assigned LCD select	I/O	3.3V	3V3
35	GPIO_EXP_3V3_P0_4	Level-shifted GPIO assigned backlight enable	I/O	3.3V	3V3
36	GPIO_EXP_3V3_P0_5	Level-shifted GPIO assigned touch shutdown	I/O	3.3V	3V3
37	GPIO_EXP_3V3_P0_6	Level-shifted GPIO assigned horizontal polarity	I/O	3.3V	3V3
38	GPIO_EXP_3V3_P0_7	Level-shifted GPIO assigned vertical polarity	I/O	3.3V	3V3
39	GND	Ground	PWR	GND	--
40	GND	Ground	PWR	GND	--
41	GND	Ground	PWR	GND	--

Table 8: LVDS Connector (J47) Pin Mapping

9.5 Network Connectivity

9.5.1 Wireless WiFi and Bluetooth

The i.MX 8M Plus Development Kit has incorporated the Azurewave AW-CM276NF wireless module to provide WiFi and Bluetooth wireless connectivity. The AW-CM276NF module provides 2.4GHz and 5GHz 802.11a/b/g/n/ac WiFi along with Bluetooth v5.3 + Bluetooth Low-Energy (BLE) functionality based on the NXP/Marvell 88W8997 chipset. The wireless module is located on the SOM and includes two I-Pex MHF4 connectors for attaching antennas. See Section 7 for instructions on connecting the antenna.

9.5.2 Wired Ethernet 10/100/1000 MAC + PHY

The i.MX 8M Plus Development Kit supports dual 10/100/1000 Mbps Ethernet.

The i.MX 8M Plus processor includes two internal Ethernet Media Access Controllers (MACs) designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. The i.MX 8M Plus SOM design completes the interface to one media with a Microchip KSZ9131 10/100/1000 PHY attached to the RGMII interface of the processor. The baseboard includes a connection to the other RGMII interface of the processor to a Microchip KSZ9131 10/100/1000 PHY.

The baseboard provides two Ethernet RJ-45 jacks with integrated magnetics. The Ethernet PHY connected to J17 is on the SOM and the Ethernet PHY connected to J50 is on the baseboard. See Figure 1 for a picture which includes the Ethernet 10/100/1000 jack at the top center.

9.5.3 Security Features

The i.MX 8M Plus SOM includes NXP’s A7101CHTK2/T0BC2VJ Plug & Trust secure element for end-to-end security.

The A71CH is a ready-to-use solution providing a root of trust at the IC level and proven, chip-to-cloud security right out of the box. It is a platform capable of securely storing and provisioning credentials, securely connecting IoT devices to cloud services and performing cryptographic node authentication.

It can be used with various host platforms and host operating systems to secure a broad range of applications.

9.6 USB Interfaces

The i.MX 8M Plus Development Kit supports USB 3.1 Gen 1 Dual Role port.

The i.MX 8M Plus processor supports two dual-role interfaces (USB1 and USB2). The USB interfaces are routed directly from the processor to the SOM Host connector.

9.6.1 USB Dual Role Port

The baseboard routes the USB1 interface from the SOM to a USB-C connector on the baseboard (J21). See Figure 1 for a picture which includes the USB-C dual-role port connector at the top edge near the center.

This USB-C port is capable of sourcing up to 1.8A, but it is limited by the amount of power pulled in from the development kit power supply.

9.6.2 USB Host Ports

The baseboard routes the USB2 interface from the SOM to a 5-port USB Hub component (U25) consisting of 3x-USB 3 host ports, 1x USB 2.0 host port and 1x USB-C port capable of USB super-speed in host-only mode on the baseboard, and one of the downstream ports is routed to the PCIe slot. The three USB 3.1 Type A receptacle connectors at locations J7, J8 and J9. The USB 2.0 Type A receptable is J6, and the USB-C host port is J22.

See Figure ***1*** for a picture which includes the three USB host port connectors along the top edge of the baseboard.

The USB host ports are mapped as follows:

- USB 3.1 Downstream Port 1 – J22 (3500mA)
- USB 3.1 Downstream Port 2 – J9 (1500mA)
- USB 3.1 Downstream Port 3 – J8 (1500mA)
- USB 3.1 Downstream Port 4 – J7 (1500mA)
- USB 3.1 Downstream Port 5 – connected to PCIe interface
- USB 2.0 Downstream Port 6 – J6 (500mA)

NOTE: All power is fed by the USB Type C input power adapter. The total system power shall not exceed the input power provided.

9.7 Audio

The following sections describes audio interfaces and features used on the development kit.

9.7.1 Synchronous audio interface (SAI)

The i.MX 8M Plus Development Kit implements four of the SOM's synchronous audio interface (SAI) modules.

- SAI1 supports 8 Tx and 8 Rx lanes but these pins are multiplexed for use for the ethernet PHY on the baseboard.
- SAI2 has been used to implement internal Bluetooth audio interface on the SOM.
- SAI3 has been used to implement the audio CODEC on the baseboard
- SAI5 has various uses on the baseboard:
    - MIPI to HDMI Transmitter
        - SCLK/MCLK
            - SAI5_RXD2 with R29 populated
        - SPDIF/I2S
            - SAI5_RXD3
        - LRCLK
            - SAI5_TXFS
    - PDM Microphone
        - SAI5_RXD0
        - SAI5_RXC
    - Expansion connector (J51)
        - SAI5_RXFS

9.7.2 Audio CODEC

The baseboard provides an Audio CODEC with 24-bit resolution from Cirrus Logic Inc., part number WM8962BECSN/R. The Audio CODEC can drive stereo headphones, drive at least one low-power speaker, and sample data from stereo line input. The Audio CODEC includes an Inter-IC Sound (I2S) interface for connection to the SOM using the SAI3 interface.

To allow full software control over all its features, the Audio CODEC supports 2-wire (I2C) serial control interface mode, with full read-back capability on all registers. The baseboard uses the SOM's I2C4 bus for this interface.

Refer to Figure ***1*** for a picture identifying the various audio connections discussed below.

9.7.2.1 Audio In/Out – Stereo Headphones

The baseboard provides a black 3.5mm audio jack at location J32 for stereo headphones. The pin mapping for the 6-pin 3.5mm stereo headphones audio jack is shown in the table below.

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain	Notes
1	MIC_RAW	Microphone In	I	1.8V	1V8_AUD	
2	HP_L	Headphone Left Channel	O	1.8V	1V8_AUD	--
3	HP_R	Headphone Right Channel	O	1.8V	1V8_AUD	--
4	AGND	Analog Ground	PWR	GND	--	--
5	RFU	--	--	--	--	--
6	GPIO_EXP_P1_1	Headphone Detect	I	3.3V	3V3_AUD	1

Table 9: 6-pin 3.5mm Stereo Headphones Jack (J32) Pin Mapping

Table Notes:

1. VREF_GPIO voltage is selectable via resistor population option on the baseboard. Populate R198 with 0-ohm resistor for 3.3V (default) or populate R207 for 1.8V.

The black 3.5mm audio jack is configured by default using the pin assignment as defined by the American Headset Jack (AHJ) standard. The baseboard can be configured to use the open mobile terminal platform (OMTP) standard by removing R458 and R459 and then populating both R460 and R457. See how the signals are assigned to the various connections of the 4-pole male end in the figure below.

Figure 15: CTIA versus OMTP

9.7.2.2 Audio Out – Stereo Line-Out

A stereo audio line-out connection is available on the baseboard at location J26. Stereo line out voltage reference default is 3.3 volts. However, there is an option of applying an external supply (5.0V) if more power is desired for stereo-line out audio.

Stereo audio line-out reference voltage selection is controlled via JP2. See Figure 11: Jumper Locations.

The pin mapping for the 4-pin stereo line-out header is shown in the table below.

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain
1	SPKRN	Speaker-out Right Channel-Negative	O	3.3/5.0V	SPKVDD
2	SPKRP	Speaker-out Right Channel-Positive	O	3.3/5.0V	SPKVDD
3	SPKLN	Speaker-out Left Channel-Negative	O	3.3/5.0V	SPKVDD
4	SPKLP	Speaker-out Left Channel-Positive	O	3.3/5.0V	SPKVDD

Table 10: 2-pin Stereo Line-Out (J26) Pin Mapping

9.7.2.3 Audio In – Stereo Line-In

A stereo audio line-in connections is available on the baseboard. The stereo line in input is available on the baseboard with a blue 3.5mm audio jack at location J27.

The pin mapping for the 6-pin 3.5mm stereo headphones audio jack is shown in the table below.

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain	Notes
1	AGND	Analog Ground	PWR	GND	--	--
2	IN4L	Left channel single-ended input 4	I	1.8V	1V8_AUD	--
3	IN4R	Right channel single-ended input 4	I	1.8V	1V8_AUD	--
4	GPIO_EXP_P1_2 (LINEIN_DET)	Microphone nDetect	I	3.3V	VREF_GPIO	1
5	RFU	--	--	--	--	--
6	RFU	--	--	--	--	--

Table 11: 6-pin 3.5mm Microphone Jack (J27) Pin Mapping

Table Notes:

1. VREF_GPIO voltage is selectable via resistor population option on the baseboard. Populate R198 with 0-ohm resistor for 3.3V (default) or populate R207 for 1.8V.

9.7.3 Pulse Density Modulation Interface

The i.MX 8M Plus Development Kit implements a Pulse Density Modulation (PDM) interface using two of the SAI5 interface bits (Rx data and clock) from the SOM.

The baseboard supports a single digital microphone over the PDM interface at location J23. The PDM interface is compatible with Knowles Mic on Flex development boards[6].

The pin mapping for the 8-pin 0.5MM FFC bottom contact ZIF connector is shown in the table below.

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain	Notes
1	RFU	--	--	--	--	--
2	DGND	Digital Ground	PWR	GND	--	--
3	POWER	3.3V/1.8V Power Out (1.8V default)	PWR	3.3/1.8V	1.8V/3.3V	1
4	SAI5_RXD0	PDM_BIT_STREAM0	I	1.8V	NVCC_1V8	
5	SAI5_RXC	PDM_CLK	I	1.8V	NVCC_1V8	
6	Select	Pull-down (default)	O	1.8V	1.8V	2
7	DGND	Digital Ground	PWR	GND	--	--
8	RFU	Reserved for Future Use	--	--	--	--

Table 12: 8-pin FFC Bottom Contact PDM Connector (J23) Pin Mapping

Table Notes:

1. PDM Voltage out is selectable via resistor population option on the baseboard. Populate R151 (default) with 0-ohm resistor for 1.8V or populate R149 for 3.3V.
2. Populate R154 with 0-ohm resistor to pull-down (default) or populate R153 to pull-up (to voltage selected in note 1.)

9.8 Camera Interface

The i.MX 8M Plus Development Kit supports two MIPI CSI-2 4-lane interfaces. The MIPI CSI-2 interfaces are routed directly from the processor to the SOM Host connector (see Section 13– Pin Descriptions & Functions).

The baseboard routes the MIPI CSI-2 interfaces from the SOM Host connector to two MIPI CSI-2 connectors (J18 and J5) on the baseboard for external camera connection. See Figure ***1***: Baseboard (Front Side) for a picture which includes the MIPI CSI-2 connectors flagged on the top side. The connectors support a 4-lane CSI-2 Interface each, with control signals delivered through an I2C bus (I2C2 & I2C4). The connector, Hirose FH41-28S-0.5SH(05), is compatible with the Basler BCON digital camera module using the Basler daA3840-30mc-IMX8MP-EVK Add-On Camera Kit[7]. The pin mapping for the MIPI CSI-2 connector on the baseboard is shown in the table below.

[6] https://www.knowles.com/subdepartment/evaluation-kits/dpt-microphones/subdpt-sisonic-surface-mount-mems
[7] https://docs.baslerweb.com/daa3840-30mc-imx8mp-evk

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain	Notes
1	DGND	Digital Ground	PWR	GND	--	--
2	MIPI_CSI1_D3_P	Differential MIPI-CSI2 data signal	I	1.8V	VDD_MIPI_1P8	--
3	MIPI_CSI1_D3_N	Differential MIPI-CSI2 data signal	I	1.8V	VDD_MIPI_1P8	--
4	DGND	Digital Ground	PWR	GND		--
5	MIPI_CSI1_D2_P	Differential MIPI-CSI2 data signal	I	1.8V	VDD_MIPI_1P8	--
6	MIPI_CSI1_D2_N	Differential MIPI-CSI2 data signal	I	1.8V	VDD_MIPI_1P8	--
7	DGND	Digital Ground	PWR	GND	--	--
8	MIPI_CSI1_CKP	Differential MIPI-CSI2 clock signal	O	1.8V	VDD_MIPI_1P8	--
9	MIPI_CSI1_CKN	Differential MIPI-CSI2 clock signal	O	GND	VDD_MIPI_1P8	--
10	DGND	Digital Ground	PWR	GND	--	--
11	MIPI_CSI1_D1_P	Differential MIPI-CSI2 data signal	I	1.8V	VDD_MIPI_1P8	--
12	MIPI_CSI1_D1_N	Differential MIPI-CSI2 data signal	I	1.8V	VDD_MIPI_1P8	--
13	DGND	Digital Ground	PWR	GND	--	--
14	MIPI_CSI1_D0_P	Differential MIPI-CSI2 data signal	I	1.8V	VDD_MIPI_1P8	--
15	MIPI_CSI1_D0_N	Differential MIPI-CSI2 clock signal	I	1.8V	VDD_MIPI_1P8	--
16	DGND	Digital Ground	PWR	GND	--	--
17	CSI_RSTN	CSI_nRST - CSI reset signal level shifted to CAM_VIO levels	I	1.8V	NVCC_GPIO1	--
18	SYNC_IN	Used to synchronize or trigger the camera (optional)	I	1.8V	--	--
19	DGND	Digital Ground	PWR	GND		--
20	I2C_SCL	I2C clock for MIPI-CSI2 camera	I/O	1.8V	1V8	--
21	I2C_SDA	I2C data for MIPI-CSI2 camera	I/O	1.8V	1V8	--
22	DGND	Digital Ground	PWR	GND	--	--
23	FLASH	Used to control external flash lighting (optional)	O	1.8V	--	--
24	SYNC_OUT	Used to synchronize multiple cameras (optional)	O	1.8V	--	--
25	VCC	Power	PWR	5V0	--	--
26	VCC	Power	PWR	5V0	--	--
27	VCC	Power	PWR	5V0	--	--
28	DGND	Digital Ground	PWR	GND	--	--

Table 13: MIPI CSI-2 Connector (J18) Pin Mapping

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain	Notes
1	DGND	Digital Ground	PWR	GND	--	--
2	MIPI_CSI2_D3_P	Differential MIPI-CSI2 data signal	I	1.8V	VDD_MIPI_1P8	--
3	MIPI_CSI2_D3_N	Differential MIPI-CSI2 data signal	I	1.8V	VDD_MIPI_1P8	--
4	DGND	Digital Ground	PWR	GND		--
5	MIPI_CSI2_D2_P	Differential MIPI-CSI2 data signal	I	1.8V	VDD_MIPI_1P8	--
6	MIPI_CSI2_D2_N	Differential MIPI-CSI2 data signal	I	1.8V	VDD_MIPI_1P8	--
7	DGND	Digital Ground	PWR	GND	--	--
8	MIPI_CSI2_CLK_P	Differential MIPI-CSI2 clock signal	O	1.8V	VDD_MIPI_1P8	--
9	MIPI_CSI2_CLK_N	Differential MIPI-CSI2 clock signal	O	GND	VDD_MIPI_1P8	--
10	DGND	Digital Ground	PWR	GND	--	--
11	MIPI_CSI2_D1_P	Differential MIPI-CSI2 data signal	I	1.8V	VDD_MIPI_1P8	--
12	MIPI_CSI2_D1_N	Differential MIPI-CSI2 data signal	I	1.8V	VDD_MIPI_1P8	--
13	DGND	Digital Ground	PWR	GND	--	--
14	MIPI_CSI2_D0_P	Differential MIPI-CSI2 data signal	I	1.8V	VDD_MIPI_1P8	--
15	MIPI_CSI2_D0_N	Differential MIPI-CSI2 clock signal	I	1.8V	VDD_MIPI_1P8	--
16	DGND	Digital Ground	PWR	GND	--	--
17	CSI2_RSTN	CSI_nRST - CSI reset signal level shifted to CAM_VIO levels	I	1.8V	NVCC_GPIO1	--
18	SYNC_IN	Used to synchronize or trigger the camera (optional)	I	1.8V	--	--
19	DGND	Digital Ground	PWR	GND		--
20	I2C_SCL	I2C clock for MIPI-CSI2 camera	I/O	1.8V	1V8	--
21	I2C_SDA	I2C data for MIPI-CSI2 camera	I/O	1.8V	1V8	--
22	DGND	Digital Ground	PWR	GND	--	--
23	FLASH	Used to control external flash lighting (optional)	O	1.8V	--	--
24	SYNC_OUT	Used to synchronize multiple cameras (optional)	O	1.8V	--	--
25	VCC	Power	PWR	5V0	--	--
26	VCC	Power	PWR	5V0	--	--
27	VCC	Power	PWR	5V0	--	--
28	DGND	Digital Ground	PWR	GND	--	--

Table 14: MIPI CSI-2 Connector (J5) Pin Mapping

9.9 UARTS

The i.MX 8M Plus Development Kit has four UART interfaces driven from the processor.

- UART1 (four-wire) – reserved for Bluetooth debug
- UART2 (two-wire) – primary use is A53 debug
- UART3 (four-wire)
- UART4 (two-wire) – primary use is M4 debug

9.9.1 UART2 and UART4 – Debug Serial Interface

The i.MX 8M Plus SOM dedicates UART2 to be used for serial communications on the Cortex-A53 processor and UART4 for the Cortex-M4 processor. Both UARTs can be designated as a debug console or be used for application purposes.

Both UART2 and UART4 are connected to a USB to Dual Port UART Converter (FTDI FT2232H) on the baseboard. The baseboard routes the USB interface from the FTDI converter chip to a USB 2.0 Micro B receptacle connector (J34) on the baseboard for external serial connection to a PC. See Figure ***1*** for a picture which includes the Debug UART USB Port flagged on the left side just below center. Typically, the Cortex-A53 appears as the lower serial port on the host PC running the terminal emulator. This serial port is used for accessing the Linux debug terminal.

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain	Notes
1	VCC5V_USB_DEBUG_IN	Receives +5V power supply from the connected device.	PWR	GND	--	--
2	USB_DEBUG_DM_R	D- is the negative data line used for transmitting data from the device to the host	I/O	5.0V	VCC5V_USB_DEBUG_IN	--
3	USB_DEBUG_DP_R	D+ is the positive data line used for transmitting data from the host to the device.	I/O	5.0V	VCC5V_USB_DEBUG_IN	--
4	RFU	Reserved for Future Use	--	--	--	--
5	DGND	Digital Ground	PWR	GND		--

Table 15: Serial Debug (J34) Pin Mapping

9.9.2 UART3 – Off-board Application Interface

UART3 is available with off-board connector options for application use. UART3 supports a 4-wire interface. It is powered by NVCC_ECSPI_HDMI which is set to 1.8V on the SOM.

UART3, at TTL voltage levels, is routed to the Expansion Connector (J37) for offboard use. Refer to Section 13 for SOM connector description and pin mapping.

UART3 is also routed to a RS-232 transceiver on the baseboard. The transceiver output is then routed to connector (J31) on the baseboard for an external RS-232 connection. See Figure ***1*** for a picture which includes the UART3 Header flagged on the center.

NOTE: The baseboard provides a Shunt Jumper (JP3) to select the desired UART3 option, TTL or RS-232. See Figure 11 for jumper location.

- *Installing the jumper forces the RS-232 transceiver to power off, to use TTL (J37).*
- *Removing the jumper energizes the RS-232 transceiver, to use RS-232 (J31).*

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain	Notes
1	RFU	Reserved for Future Use	--	--	--	--
2	RFU	Reserved for Future Use	--	--	--	--
3	RSA_RXD	RS-232 receive	I	3.3V	3V3	--
4	RSA_RTS	RS-232 request to send	O	3.3V	3V3	--
5	RSA_TXD	RS-232 transmit	O	3.3V	3V3	--
6	RSA_CTS	RS-232 clear to send	I	3.3V	3V3	--
7	RFU	Reserved for Future Use	--	--	--	--
8	RFU	Reserved for Future Use	--	--	--	--
9	DGND	Digital Ground	PWR	GND		--
10	DGND	Digital Ground	PWR	GND		--

Table 16: UART3 (J31) Pin Mapping

9.10 SPI

The i.MX 8M Plus Development Kit has an Enhanced Configurable Serial Peripheral Interfaces (ECSPI) extended from the processor. The SPI interface can be operated as either master or slave.

- ECSPI2

9.10.1 ECSPI2 – TPM

ECSPI2 from the SOM is routed to a SPI TPM on the baseboard.

ECSPI2 from the SOM is also available on the Expansion connector (J37) for application use. Refer to Table 21 for the pin mapping of the expansion connector.

9.11 I2C

The i.MX 8M Plus Development Kit has four Inter-Integrated Circuit (I2C) interfaces from the processor.

- I2C1
- I2C2
- I2C3
- I2C4

Using the software provided by Beacon EmbeddedWorks, the controllers default to 384 KHz operation. The NVCC_I2C_UART rail is fixed to +1.8V operation; the SOM uses this power rail to supply power to all I2C devices on the bus. Host designers must keep this in mind if attaching any devices to the I2C bus.

9.11.1 I2C1 – SOM PMIC Interface

The I2C1 interface is dedicated to the PMIC on the SOM.

9.11.2 I2C2 – Baseboard Functions and Off-board Expansion

The I2C2 interface is routed directly from the processor to the SOM Host connector (see Section 13 for SOM connection descriptions and pin mapping).

The baseboard uses the I2C2 interface from the SOM for several baseboard functions:

- GPIO Expanders
- MIPI DSI to HDMI transmitter control/status
- External LVDS Touchscreen control/status
- PCIe Clock Generator
- CSI Camera (MIPI CSS1)

The I2C2 interface connects to J46 for LCD support and U34 for PCIe support. The I2C2 interface is converted to 3V3 levels through U35.

The I2C2 interface connects to one MIPI CSI-2 camera interface (J18). These I2C2 signals are 1.8V compatible.

The I2C2 interface is also routed to an expansion connector (J37) for application use. The signals connected to J37 are 3.3V compatible.

9.11.3 I2C3 – SOM Functions and Off-board Expansion

The I2C3 interface is used to communicate/control the following SOM functions:

- Manufacturing EEPROM
- Real-time clock
- Security Chip

The baseboard uses the I2C3 interface from the SOM for several baseboard functions:

- USB Type C Power Delivery (PD) PHY (x2)

Refer to Section 9.15.2 for SOM connector description and pin mapping.

9.11.4 I2C4 – Off-board Expansion

The I2C4 interface is routed directly from the processor to the SOM Host connector (see Section 13 for SOM connector descriptions and pin mappings).

The I2C4 interface is used to communicate/control the following baseboard functions:

- Audio CODEC (three separate addresses)
- GPIO Expander (x2)
- External LVDS Touchscreen control/status
- USB-C Port Mux
- CSI Camera (MIPI CSS2)

Refer to Section 13 for SOM connector description and pin mapping.

9.11.5 Address Mapping for I2C Busses

The table below shows the address mapping for all the I2C buses.

I2C Bus	Device	Ref Designator	Address	Note
I2C1	Power Management IC	SOM: U3	0100101b (0x25)	--
I2C2	LVDS0 Touch	Baseboard: J46	0100110b (0x26)	--
I2C2	LVDS0 Touch	Baseboard: J46	1100010 (0x62)	**2**
I2C2	DSI to HDMI	Baseboard: U11	1111000b (0x38) 1111011b (0x3c) 1110010b (0x3d) 1111111b (0x3f)	--
I2C2	PCIe Clock Generator	Baseboard: U34	1101000b (0x68)	--
I2C2	MIPI_CSI 1	Baseboard: J18	Camera Defined	**1**
I2C2	GPIO Header	Baseboard: J37	User Def	--
I2C2	GPIO Expander	Baseboard: U27	0100000 (0x20)	--
I2C3	Manufacturing EEPROM	SOM: U6	1010000b (0x50)	--
I2C3	RTC	SOM: U9	1010001b (0x51)	--
I2C3	Security IC	SOM: U7	1001000b (0x48)	--
I2C3	CC Logic Det	Baseboard: U54	1010011 (0x53)	--
I2C3	CC Logic Det	Baseboard: U73	1010010 (0x52)	--
I2C4	LVDS1 Touch	Baseboard: J47	0100110b (0x26)	--
I2C4	LVDS1 Touch	Baseboard: J46	1100010 (0x62)	**2**
I2C4	Audio CODEC	Baseboard: U32	0011010b (0x1A)	--
I2C4	Audio CODEC	Baseboard: U32	1001010b (0x4A)	**2**
I2C4	Audio CODEC	Baseboard: U32	1101001b (0x69)	**2**
I2C4	GPIO Expander	Baseboard: U44	0100000b (0x20)	--
I2C4	GPIO Expander	Baseboard: U30	0100001b (0x21)	--
I2C4	MIPI_CSI 2	Baseboard: J5	Camera Defined	**1**
I2C4	USB-C Port MUX	Baseboard: U13	1000111 (0x47)	--

NOTE:
1. Resister population option for MIPI camera I2C port
2. Reserved

Table 17: Address Mappings for I2C Busses

9.12 PCIe M.2

The i.MX 8M Plus Development Kit provides PCI Express Gen 3 functionality, single lane. The baseboard receives one single-lane PCIe Gen 3 interface from the SOM host connector (see Section 13 – Pin Descriptions & Functions) and routes it through a selector to choose between M.2 Key B (J48) and M.2 Key M (J45). Both sockets are on the backside of the baseboard.

9.12.1 PCIe M.2 Key B (J48) Pin Mapping

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain	Notes
1	PCIE_B_CONFIG_3	PCIe Config 3	I/O	3.3V	3V3_PCIE_B	--
2	3V3_PCIE_B	PWR	--	3.3V	3V3	--
3	DGND	PWR	--	GND	--	--
4	3V3_PCIE_B	PWR	--	3.3V	3V3	--
5	DGND	PWR	--	GND	--	--
6	CAT6_POWER_OFFN	Full Card Power Off	I/O	3.3V	3V3	--
7	USB2.5_DP	USB Data+	I/O	Variable	--	2
8	W_DISABLE1N	W_nDisable	I/O	3.3V	3V3	--

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain	Notes
9	USB2.5_DM	USB Data-	I/O	Variable	--	2
10	W_LED	LED		3.3V	3V3_PCIE_B	--
11	DGND	PWR	--	GND	--	--
20	I2S_CLK	I2S Clock; connected to J20.10	O	1.8V	--	--
21	PCIE_B_CONFIG_0	PCIe Config 0	I/O	3.3V	3V3_PCIE_B	--
22	PCM_IN	PCM_IN; connected to J20.7	I	1.8V	--	--
23	WAKE_ON_WANN_1V8		I/O	1.8V		--
24	NC_PCM_OUT	PCM_OUT; connected to J20.9	O	1.8V	--	--
25	DPR	Dynamic power reduction	O	1.8V/3.3V	1V8/3V3_PCIE_B	--
26	GNSS_EN	GNSS Enable	O	3.3V	3V3_PCIE_B	--
27	DGND	PWR	--	GND	--	--
28	PCM_SYNC	PCM data frame sync; connected to J20.5	I/O	User Define	--	--
29	USB2.5_RXM	USB RX-	I	Variable	--	2
30	USIM1_RESET	SIM1 reset	I	1.8/3.0V	USIM1_VDD	--
31	USB2.5_RXP	USB RX+	I	Variable	--	2
32	USIM1_CLK	SIM1 clock	I	1.8/3.0V	USIM1_VDD	--
33	DGND	PWR	--	GND	--	
34	USIM1_DATA	SIM1 Data	I/O	1.8/3.0V	USIM1_VDD	--
35	USB2.5_TXM_1	USB TX-1	O	Variable	--	2
36	USIM1_VDD	PWR	--	1.8/3.0V	USIM1_VDD	--
37	USB2.5_TXP_1	USB TX+1	O	Variable	--	2
38	--	--	--	--	--	--
39	DGND	PWR	--	GND	--	--
40	USIM2_DET	SIM2 insertion detection	O	1.8/3.0V	USIM2_VDD	
41	PCIE_B_RXN	PCIe RX-	I	Variable	VDDA_1V8	1
42	USIM2_DATA	SIM2 Data	I/O	1.8/3.0V	USIM2_VDD	--
43	PCIE_B_RXP	PCIe RX+	I	Variable		1
44	USIM2_CLK	SIM2 CLK	I	1.8/3.0V	USIM2_VDD	--
45	DGND	PWR	--	GND	--	--
46	USIM2_RESET	SIM2 Reset	I	1.8/3.0V	USIM2_VDD	--
47	PCIE_B_TXN	PCIe TX-	O	Variable	VDDA_1V8	1
48	USIM2_VDD	PWR	--	1.8/3.0V	USIM2_VDD	--
49	PCIE_B_TXP	PCIe TX+	O	Variable	VDDA_1V8	1
50	CELLMOD_RESETN	PCIe nReset	O	3.3V	3V3_PCIE_B	--
51	DGND	PWR	--	GND	--	--
52	PCIE_B_NCLKREQ_DEV	PCIe Clock nRequest	I/O	3.3V	3V3_PCIE_B	

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain	Notes
53	PCIE_B_REF_CLKN	PCIe Clock-	O	Variable	VDDA_1V8	1
54	PCIEWAKEN	PCIe nWake	I/O	3.3V	3V3_PCIE_B	--
55	PCIE_B_REF_CLKP	PCIe Clock+	O	Variable	VDDA_1V8	1
56	I2C_SDA_AUDIO	I2C data used for external codec; connected to J20.1	I/O	User Define	User Define	--
57	DGND	PWR	--	GND		--
58	I2C_SCL_AUDIO	I2C clock used for external clock; connected to J20.3	I	User Define	User Define	--
59	ANTCTL0	Antenna tuner control; connected to J20.2	I	User Define	User Define	--
60	--	--	--	--	--	--
61	ANTCTL1	Antenna tuner control; connected to J20.4	I	User Define	User Define	--
62	--	--	--	--	--	--
63	ANTCTL2	Antenna tuner control; connected to J20.6	I	User Define	User Define	--
64	--	--	--	--	--	--
65	ANTCTL3	Antenna tuner control; connected to J20.8	I	User Define	User Define	--
66	USIM1_DET	SIM1 Detect	O	User Define	USIM1_VDD	--
67	CELLMOD_PRESET	NC	--	--1.8V	--	--
68	ANT_CONFIG	NC	--	--	--	--
69	PCIE_B_CONFIG_1	NC	--	--	--	--
70	3V3_PCIE_B	PWR	--	3.3V	3V3	--
71	DGND	PWR	--	GND	--	--
72	3V3_PCIE_B	PWR	--	3.3V	3V3	--
73	DGND	PWR	--	GND	--	--
74	3V3_PCIE_B	PWR	--	3.3V	3V3	--
75	PCIE_B_CONFIG_2	NC	--	--	--	--

Note:

1. PCIe voltage levels follow the PCIe specification and depend on the operating speed. Please see PCI-SIG for more information.
2. USB voltage levels follow the USB specification and depend on the USB operating speed. Please see the USB Specification for more information.

Table 18: M.2 Key B (J48) Pin Mapping

9.12.2 PCIe M.2 Key M (J45) Pin Mapping

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain	Notes
1	PCIE_M_CONFIG_3	PCIe Config 3	I/O	GND	--	--
2	3V3_PCIE_M	PWR	--	3.3V	3V3	--
3	DGND	PWR	--	GND	--	--
4	3V3_PCIE_M	PWR	--	3.3V	3V3	--
5	--	--	--	--	--	--

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain	Notes
6	--	--	--	--	--	--
7	--	--	--	--	--	--
8	--	--	--	--	--	--
9	DGND	PWR	--	GND	--	
10	--	--	--	--	--	--
11	--	--	--	--	--	--
12	3V3_PCIE_M	PWR		3.3V	3V3	--
13	--	--	--	--	--	--
14	3V3_PCIE_M	PWR	--	3.3V	3V3	--
15	DGND	PWR	--	GND	--	--
16	3V3_PCIE_M	PWR		3.3V	3V3	--
17	--	--	--	--	--	--
18	3V3_PCIE_M	PWR		3.3V	3V3	
19	--	--	--	--	--	--
20	--	--	--	--	--	--
21	PCIE_M_CONFIG_0	PCIe Config 0	I/O	GND	--	--
22	--	--	--	--	--	--
23	--	--	--	--	--	--
24	--	--	--	--	--	--
25	--	--	--	--	--	--
26	--	--	--	--	--	--
27	DGND	PWR	--	GND	--	--
28	--	--	--	--	--	--
29	--	--	--	--	--	--
30	--	--	--	--	--	--
31	--	--	--	--	--	--
32	--	--	--	--	--	--
33	DGND	PWR	--	GND	--	
34	--	--	--	--	--	--
35	--	--	--	--	--	--
36	--	--	--	--	--	--
37	--	--	--	--	--	--
38	SSD_DEV_SLP	Device Disable	I/O	3.3V	3V3_PCIE_M	--
39	DGND	PWR	--	GND	--	--
40	--	--	--	--	--	--
41	PCIE_M_RXN	PCIe RX-		Variable	VDDA_1V8	1
42	--	--	--	--	--	--
43	PCIE_M_RXP	PCIe RX+		Variable	VDDA_1V8	1
44	--	--	--	--	--	--
45	DGND	PWR	--	GND	--	

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain	Notes
46	--	--	--	--	--	--
47	PCIE_M_TXN	PCIe TX-		Variable	VDDA_1V8	1
48	--	--	--	--	--	--
49	PCIE_M_TXP	PCIe TX+		Variable	VDDA_1V8	1
50	SSD_RESETN	SSD Reset	I/O	3.3V	3V3	--
51	DGND	PWR	--	GND	--	--
52	PCIE_M_NCLKREQ_DEV	PCIe Clock Request	I/O	3.3V	3V3	--
53	PCIE_M_REF_CLKN	PCIe Clock -		Variable	VDDA_1V8	1
54	PEWAKEN_R	PCIe nWake	I/O	3.3V	3V3	--
55	PCIE_M_REF_CLKP	PCIe Clock +		Variable	VDDA_1V8	1
56	--	--	--	--	--	--
57	DGND	PWR	--	GND	--	
58	--	--	--	--	--	--
67	--	--	--	--	--	--
68	SUSCLK	NC	--	--	--	--
69	PCIE_M_CONFIG_1	PCIe Config 1	I/O	GND	--	--
70	3V3_PCIE_M	PWR	--	3.3V	3V3	--
71	DGND	PWR	--	GND	--	--
72	3V3_PCIE_M	PWR	--	3.3V	3V3	--
73	DGND	PWR	--	GND	--	--
74	3V3_PCIE_M	PWR	--	3.3V	3V3	--
75	PCIE_M_CONFIG_2	PCIe Config 2	I/O	GND	--	--

Note:

1. PCIe voltage levels follow the PCIe specification and depend on the operating speed. Please see PCI-SIG for more information.

Table 19: PCIe – M.2 Key M (J45) Pin Mapping

9.13 RTC

The i.MX 8M Plus Development Kit provides an ultra-low power real-time clock (RTC).

The RTC resides on the SOM and communicates to the processor on the I2C3 bus. The RTC receives battery backup from a coin cell battery on the baseboard. The baseboard also includes a shunt jumper (JP1), which is populated by default, to enable the coin cell battery to charge when the Development Kit is powered up.

9.14 General Purpose I/O

9.14.1 SOM GPIO

The i.MX 8M Plus processor has over 87 multiplexed GPIOs supporting various peripherals such as PWMs, SDIO, UART, SPI, and I2C. The i.MX 8M Plus SOM incorporates many of the GPIOs into the design. The SOM extends some GPIO to the baseboard.

GPIO assignments used appear in the “Signal Name” column, while the “Processor Alternate Functions” column shows what other GPIO selections would have been possible.

9.14.2 Baseboard GPIO Expansion

In addition to the GPIO signals extended from the SOM, the baseboard adds further GPIO options by incorporating two 16-bit GPIO Expanders, one at 3.3V I/O levels and the other at 1.8V. Both share the same interrupt line (SAI2_MCLK).

Component Designator	Source Bus	ADDR Input	Slave Address	Signal Name	Functions
U44	I2C4	GND	0x20h	GPIO_EXP_3V3_P0_0 GPIO_EXP_3V3_P0_1 GPIO_EXP_3V3_P0_2 GPIO_EXP_3V3_P0_3 GPIO_EXP_3V3_P0_4 GPIO_EXP_3V3_P0_5 GPIO_EXP_3V3_P0_6 GPIO_EXP_3V3_P0_7 GPIO_EXP_3V3_P1_0 GPIO_EXP_3V3_P1_1 GPIO_EXP_3V3_P1_2 GPIO_EXP_3V3_P1_3 GPIO_EXP_3V3_P1_4 GPIO_EXP_3V3_P1_5 GPIO_EXP_3V3_P1_6 GPIO_EXP_3V3_P1_7	Port 0 – GPIO_EXP_3V3 Bit 0 Port 0 – GPIO_EXP_3V3 Bit 1 Port 0 – GPIO_EXP_3V3 Bit 2 Port 0 – GPIO_EXP_3V3 Bit 3 Port 0 – GPIO_EXP_3V3 Bit 4 Port 0 – GPIO_EXP_3V3 Bit 5 Port 0 – GPIO_EXP_3V3 Bit 6 Port 0 – GPIO_EXP_3V3 Bit 7 Port 1 – GPIO_EXP_3V3 Bit 0 Port 1 – GPIO_EXP_3V3 Bit 1 Port 1 – GPIO_EXP_3V3 Bit 2 Port 1 – GPIO_EXP_3V3 Bit 3 Port 1 – GPIO_EXP_3V3 Bit 4 Port 1 – GPIO_EXP_3V3 Bit 5 Port 1 – GPIO_EXP_3V3 Bit 6 Port 1 – GPIO_EXP_3V3 Bit 7
U30	I2C4	VDD	0x21h	GPIO_EXP_P0_0 GPIO_EXP_P0_1 GPIO_EXP_P0_2 GPIO_EXP_P0_3 GEN_LED0 GEN_LED1 GEN_LED2 GPIO_EXP_P0_7 GPIO_EXP_P1_0 GPIO_EXP_P1_1 GPIO_EXP_P1_2 GPIO_EXP_P1_3 P1_4 – GEN_BTN0 P1_5 – GEN_BTN1 P1_6 – GEN_BTN2 P1_7 – GEN_BTN3	Port 0 (0) – USB1_PWEN Port 0 (1) – USB1_OVC Port 0 (2) – PCIE_nCLKREQ Port 0 (3) – WATTSON_INT Port 0 (4) – General LED0 Port 0 (5) – General LED1 Port 0 (6) – General LED2 Port 0 (7) – USB_HUB_RESETn Port 1 (0) – Test Point 162 Port 1 (1) – HEADPHONE_DET Port 1 (2) – LINEIN_DET Port 1 (3) – CODEC_PWR_EN Port 1 (4) – General Button 0 Port 1 (5) – General Button 1 Port 1 (6) – General Button 2 Port 1 (7) – General Button 3

U27	I2C2	GND	0x20h	GPIO2_EXP_3V3_P0_0 GPIO2_EXP_3V3_P0_1 GPIO2_EXP_3V3_P0_2 GPIO2_EXP_3V3_P0_3 GPIO2_EXP_3V3_P0_4 GPIO2_EXP_3V3_P0_5 GPIO2_EXP_3V3_P0_6 GPIO2_EXP_3V3_P0_7 GPIO2_EXP_3V3_P1_0 LVDS0_TCH_INT LVDS1_TCH_INT TCPC_nINT GPIO2_EXP_3V3_P1_4 GPIO2_EXP_3V3_P1_5 GPIO2_EXP_3V3_P1_6 GPIO2_EXP_3V3_P1_7	Port 0 (0) – PEWAKEn_R Port 0 (1) – PCIE_M_nCLKREQ_DEV Port 0 (2) – SSD_RESETn Port 0 (3) – PCIEWAKEn Port 0 (4) – PCIE_B_nCLKREQ_DEV Port 0 (5) – W_DISABLE1n Port 0 (6) – CAT6_POWER_OFFn Port 0 (7) – USB_HUB_nRESET Port 1 – GPIO_EXP_3V3 Bit 0 Port 1 – GPIO_EXP_3V3 Bit 1 Port 1 – GPIO_EXP_3V3 Bit 2 Port 1 – GPIO_EXP_3V3 Bit 3 Port 1 – GPIO_EXP_3V3 Bit 4 Port 1 – GPIO_EXP_3V3 Bit 5 Port 1 – GPIO_EXP_3V3 Bit 6 Port 1 – GPIO_EXP_3V3 Bit 7

Table 20: Pin Mappings for I2C GPIO Expanders

9.15 Expansion Headers

The i.MX 8M Plus Development Kit provides two 40-pin headers on the baseboard for expansion, application development and test labeled J33, and J37. There is also a 10-pin header for miscellaneous expansion labeled J51.

9.15.1 J37 GPIO Expansion Header

The baseboard includes a GPIO Expansion Header at location J37. The baseboard routes several GPIO signals from the U44 GPIO Expander. See Figure ***1*** for a picture which includes the J37 GPIO header on the lower left quadrant. In addition to GPIO, the header also supports an I2C bus (I2C2_3V3), UART (UART3) and SPI bus (ECSPI2).

The pin mapping for the 40-pin (2x20) GPIO expansion header connector is shown below.

Pin#	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain
1	3V3	3.3V logic power supply	PWR	3.3V	3V3_IN
2	5V0	5.0V Logic power supply	PWR	5.0V	5V0_IN
3	I2C2_SDA_3V3	I2C-2 data (3.3V levels)	I/O	3.3V	3.3V
4	5V0	5.0V Logic power supply	PWR	5.0V	5V0_IN
5	I2C2_SCL_3V3	I2C-2 clock (3.3V levels)	O	3.3V	3.3V
6	DGND	Ground	PWR	GND	--
7	UART3_CTS	UART3 CTS	I	3.3V	NVCC_1V8_3V3_SW
8	UART3_TXD	UART3 TX	O	3.3V	NVCC_1V8_3V3_SW
9	DGND	Ground	PWR	GND	--
10	UART3_RXD	UART3 RX	I	3.3V	NVCC_1V8_3V3_SW
11	UART3_RTS	UART3 RTS	O	3.3V	NVCC_1V8_3V3_SW
12	GPIO_EXP_3V3_P0_0	GPIO Expansion P0-0	I/O	3.3V	3V3
13	GPIO_EXP_3V3_P0_1	GPIO Expansion P0-1	I/O	3.3V	3V3
14	DGND	Ground	PWR	GND	--
15	GPIO_EXP_3V3_P0_2	GPIO Expansion P0-2	I/O	3.3V	3V3
16	GPIO_EXP_3V3_P0_3	GPIO Expansion P0-3	I/O	3.3V	3V3
17	3V3	3.3V logic power supply	PWR	3.3V	3V3_IN
18	GPIO_EXP_3V3_P0_4	GPIO Expansion P0-4	I/O	3.3V	3V3
19	ECSPI2_MOSI	SPI2 MOSI	I/O	3.3V	NVCC_1V8_3V3_SW
20	DGND	Ground	PWR	GND	--
21	ECSPI2_MISO	SPI2 MISO	I/O	3.3V	NVCC_1V8_3V3_SW
22	GPIO_EXP_3V3_P0_5	GPIO Expansion P0-5	I/O	3.3V	3V3
23	ECSPI2_SCLK	SPI2 SCLK	O	3.3V	NVCC_1V8_3V3_SW
24	No Connect	By default, this is a no connect signal; if R285 is populated this can be UART3_RTS but is shared by other interfaces; please refer to the baseboard schematics for more information on shared usage	O	3.3V	NVCC_1V8_3V3_SW
25	DGND	Ground	PWR	GND	--
26	GPIO_EXP_3V3_P0_6	GPIO Expansion P0-6	I/O	3.3V	3V3
27	RFU	Reserved for future use	--	--	--
28	RFU	Reserved for future use	--	--	--
29	GPIO_EXP_3V3_P0_7	GPIO Expansion P0-7	I/O	3.3V	3V3
30	DGND	Ground	PWR	GND	--
31	GPIO_EXP_3V3_P1_0	GPIO Expansion P1-0	I/O	3.3V	3V3
32	GPIO_EXP_3V3_P1_1	GPIO Expansion P1-1	I/O	3.3V	3V3
33	GPIO_EXP_3V3_P1_2	GPIO Expansion P1-2	I/O	3.3V	3V3
34	DGND	Ground	PWR	GND	--
35	GPIO_EXP_3V3_P1_3	GPIO Expansion P1-3	I/O	3.3V	3V3
36	GPIO_EXP_3V3_P1_4	GPIO Expansion P1-4	I/O	3.3V	3V3

37	GPIO_EXP_3V3_P1_5	GPIO Expansion P1-5	I/O	3.3V	3V3
38	GPIO_EXP_3V3_P1_6	GPIO Expansion P1-6	I/O	3.3V	3V3
39	DGND	Ground	PWR	GND	--
40	GPIO_EXP_3V3_P1_7	GPIO Expansion P1-7	I/O	3.3V	3V3

Table 21: GPIO Expansion Header (J37) Pin Mapping

9.15.2 J51 Miscellaneous Interface Expansion Header

The baseboard includes a miscellaneous Interface Expansion Header at location J51. The baseboard routes several interface signals from the SOM Host connector to the 10-pin interface header. See Figure ***1*** for a picture which includes the J51 miscellaneous interface header flagged right side and seen on the baseboard in the bottom center.

The pin mapping for the 10-pin (2x5) expansion header connector is shown in the table below.

Pin#	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain
1	SAI5_RXFS	SAI5_RXFS	I/O	1.8V	NVCC_1V8
2	EARC_AUX	EARC_AUX	I/O	1.8V	VDDA_1V8
3	SAI1_RXC	SAI1_RXC	O	1.8V	1V8
4	UART1_TXD[1]	UART1 TXD	O	1.8V	NVCC_1V8
5	SPDIF_RX	CAN Rx	I	1.8V	NVCC_1V8
6	UART1_RXD[2]	UART1 RXD	I	1.8V	NVCC_1V8
7	GPIO1_IO11	USB-C ABI	O	1.8V	3V3_GATED
8	GPIO2_IO10	GPIO2_IO10	I/O	1.8V	NVCC_1V8
9	GPIO2_EXP_3V3_P1_0	GPIO2_EXP_3V3_P1_0	I/O	3.3V	3V3
10	DGND	Ground	PWR	GND	--

Notes:

1. Signal is floating unless R578 is populated
2. Signal is floating unless R579 is populated

Table 22: Miscellaneous Interface Expansion Header (J51) Pin Mapping

9.15.3 J33 Power/Clocks Expansion Header

The baseboard includes a Power/Clocks Expansion Header at location J33. The baseboard routes several power and clock signals from the SOM Host connector to the 40-pin power/clocks expansion header. See Figure ***1*** for a picture which includes the J33 power/clocks header seen below the SOM. In addition to various SOM power, processor and ethernet clock signals, the header also supports interrupts and power-on reset.

The pin mapping for the 40-pin (2x20) J33 power/clocks header is shown in the table below.

Pin#	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain
1	LDO5	SOM LDO4	PWR	0.8 to 3.3V	VSYS
2	NVCC_SD2	SOM NVCC_SD2	PWR	3.3 or 1.8V	NVCC_3V3 or NVCC_1V8
3	--	--	--	--	--
4	VDD_ARM_0V9	SOM VDD_ARM_0V9	PWR	0.9V	See Note 1
5	NVCC_DRAM_1V1	SOM NVCC_DRAM_1V1	PWR	1.1V	See Note 1
6	VDD_SNVS_0V8	SOM VDD_SNVS_0V8	PWR	0.8V	See Note 1
7	NVCC_1V8	SOM NVCC_1V8	PWR	1.8V	NVCC_1V8
8	VDD_SOC_0V8	SOM VDD_SOC_0V8	PWR	0.82V	See Note 1
9	NVCC_3V3	SOM NVCC_3V3	PWR	3.3V	NVCC_3V3
10	NVCC_SNVS_1V8	SOM NVCC_SNVS_1V8	PWR	1.8V	See Note 1
11	VDDA_1V8	SOM VDDA_1V8	PWR	1.8V	See Note 1
12	VDD_PHY_0V9	SOM VDD_PHY_0V9	PWR	0.9V	See Note 1
13	VDD_DRAM&PU_0V9	SOM VDD_DRAM&PU_0V9	PWR	0.9V	See Note 1
14	VDD_PHY_1V2	SOM VDD_PHY_1V2	PWR	1.2V	See Note 1
15	NVCC_SAI	SOM NVCC_SAI	PWR	1.8V	See Note 1
16	BT_LED	BT_LED	I/O	1.8V	NVCC_1V8_WLAN
17	NVCC_ECSPI	SOM NVCC_ECSPI	PWR	3.3V	See Note 1
18	WLAN_LED	WLAN_LED	I/O	1.8V	NVCC_1V8_WLAN
19	GPIO1_IO12	GPIO1 IO12	I/O	1.8V	Floating
20	32KOUT	32KOUT	--	--	
21	RTC_NINTA	RTC Interrupt	I	1.8V	NVCC_1V8
22	JTAG_MOD	JTAG_MOD	I	1.8V	NVCC_1V8
23	DGND	Ground	PWR	GND	--
24	NPOR	POWER ON RESET	OD	1.8V	NVCC_SNVS_1P8
25	CLKOUT1	CLKOUT1	O	1.8V	NVCC_1V8
26	PMIC_NINT	PMIC Interrupt	I/O, OD	1.8V	NVCC_1V8
27	DGND	Ground	PWR	GND	--
28	DGND	Ground	PWR	GND	--
29	CLKOUT2	CLKOUT2	O	1.8V	NVCC_1V8
30	CLKIN1	CLKIN1	I	1.8V	NVCC_1V8
31	DGND	Ground	PWR	GND	--
32	DGND	Ground	PWR	GND	--
33	WLAN_COEX_SOUT	WLAN_COEX_SOUT	I/O	1.8V	NVCC_1V8_WLAN
34	CLKIN2	CLKIN2	I	1.8V	NVCC_1V8
35	DGND	Ground	PWR	GND	--
36	DGND	Ground	PWR	GND	--
37	ENET_XTLI	ENET_XTLI	IA	1.2	Floating from SOM
38	WLAN_COEX_SIN	WLAN_COEX_SIN	I/O	1.8V	NVCC_1V8_WLAN
39	DGND	Ground	PWR	GND	--
40	DGND	Ground	PWR	GND	--

Table 23: Power/Clocks Expansion Header (J33) Pin Mapping

TABLE NOTES:

1. Power supply is not routed by default (resistor not populated) as it is only for debug and should not be connected or used

9.16 User Buttons

The i.MX 8M Plus baseboard provides several user buttons. The functionality of each user button is outlined in the table below. See section 10.1 Boot Configuration and Modes for how to set S2 to configure the desired boot mode.

Button	Switch Type	Signal Name	Function (Plus)
S3	Tactile SPST, Momentary	SYS_nRST	System Reset
S6	Slide SPDT	MAIN_IN	Main Power Switch
S7	Tactile SPST, Momentary	GEN_BTN0	General Button 0
S8	Tactile SPST, Momentary	GEN_BTN1	General Button 1
S9	Tactile SPST, Momentary	GEN_BTN2	General Button 2
S10	Tactile SPST, Momentary	GEN_BTN3	General Button 3
S4	Tactile SPST, Momentary	nPOR	Master Reset
S5	Tactile SPST, Momentary	ONOFF	SOM Power On/Off
S2	DIP, 8 SPST, Rocker	SwSeg1 - BOOT_MODE0 SwSeg2 - BOOT_MODE1 SwSeg3 – BOOT_MODE2 SwSeg4 – BOOT_MODE3 SwSeg5 - NC SwSeg6 - NC SwSeg7 - NC SwSeg8 - NC	BOOT_MODE0 BOOT_MODE1 BOOT_MODE2 BOOT_MODE3 No Connect No Connect No Connect No Connect

Table 24: Baseboard User Buttons

9.17 LEDs

The i.MX 8M Plus baseboard provides several Light Emitting Diodes (LEDs).

Reference	Description	Color	Notes
D5	J22 - USB2_VBUS	Green	--
D6	J45 – 3V3_PCIE_M	Green	--
D13	J48 - 3V3_PCIE_B	Green	--
D11	J48 - W_LED	Green	---
D30	LED0, U30 - GEN_LED0	Green	See Baseboard GPIO Expander
D31	LED1, U30 - GEN_LED1	Green	See Baseboard GPIO Expander
D32	LED2, U30 - GEN_LED2	Green	See Baseboard GPIO Expander
D33	LED3, SOM. SAI3_RXFS	Green	ALT5_GPIO4_IO28
D34	1.8V Power ON	Green	--
D43	3.3V Power ON	Green	--
D40	5V Power ON	Green	--
D25	U83 - FTDI_nRXLEDA	Green	--
D24	U83 - FTDI_nTXLEDA	Orange	--
D27	U83 - FTDI_nRXLEDB	Green	--
D26	U83 - FTDI_nTXLEDB	Orange	--

Table 25: Baseboard LEDs

10 System Integration

10.1 Boot Configuration and Modes

The i.MX 8M Plus SOM provides access to four i.MX 8M Plus boot mode pins, BOOT_MODE0 through BOOT_MODE3, through the off-board connectors. The BOOT_MODE pins are

referenced to NVCC_JTAG which is tied to +1.8V and are set using S2 on the baseboard. The i.MX 8M Plus processor provides internal pull-downs that bias the BOOT_MODE[3:0] pins to "0000" that defaults booting from the fuse settings.

Ref Designator	Signal	i.MX 8M Plus Pad Name (Pin)	Notes
J2.24	BOOT_MODE0	BOOT_MODE0 (G10)	—
J2.26	BOOT_MODE1	BOOT_MODE1 (F8)	—
J3.85	BOOT_MODE2	BOOT_MODE2 (G8)	—
J3.84	BOOT_MODE3	BOOT_MODE3 (G12)	—

Table 26: i.MX 8M Plus Boot Mode Pins

Table 27: i.MX 8M Plus Boot Mode Settings below describes the available boot modes on the i.MX 8M Plus. Please refer to "Section 6.1.2" of *i.MX 8M Plus Applications Processor Reference Manual* for further details. Note that the BOOT_MODE[3:0] pins are sampled on the rising edge of the nPOR pin. The boot mode signal can be configured using S2 on the baseboard.

BOOT_MODE[3:0] / S2 (4:1)	Boot Type	Notes
0000	Boot From Fuses	1
0001	USB Serial Downloader	2
0010	uSDHC3 / SOM eMMC	—
0011	uSDHC2 / Baseboard uSD	—
0110	SOM QSPI Flash	—

Table 27: i.MX 8M Plus Boot Mode Settings

TABLE NOTES:

1. Default boot mode based on internal pull-down resistors in the i.MX 8M Plus processor.
2. From the i.MX 8M Plus Reference Manual: "ROM supports both USB ports on the chip for boot purposes. Only one port can be selected as the boot connection. The port that is active first wins the selection." The i.MX 8M Plus Development Kit supports proper USB boot from J21, but custom designs should keep this note in mind if using a different USB configuration.

10.2 Resets

10.2.1 Power-on Reset

The i.MX 8M Plus SOM takes advantage of the integration NXP provides between the PMIC and the i.MX 8M Plus processor for power sequencing and reset. The i.MX 8M Plus contains an internal System Reset Controller (SRC) that interacts directly with pins provided by the PMIC to properly power up the processor. Power-on Reset (nPOR) is an output (open-drain) from the PMIC to the processor.

The baseboard is also able to drive nPOR via the S4 button switch. This is not a typical use case as it will only reset the processor and not the PMIC. Therefore, this could leave the PMIC in a different state than what it would be out of power-on reset.

10.2.2 System Reset

The i.MX 8M Plus baseboard drives System Reset (SYS_nRST) via the S3 button switch. The S3 button switch is connected to the power button input (PMIC_RST_B) of the PMIC for triggering the PMIC to reset. System reset is considered the main reset for the development kit.

10.3 Interrupts

The i.MX 8M Plus SOM provides many of the GPIO pins that can serve as external interrupt sources to the i.MX 8M Plus. "Table 7-1" in "Section 7.1.2" of the *i.MX 8M Plus Applications Processor Reference Manual* describes supported A53 Interrupts. Many of these are peripheral/controller related while others are associated with GPIO, which are typically IRQs 56-73.

Many of the i.MX 8M Plus multiplexed pins can be configured as GPIO which can be assigned as an interrupt source. "Section 8" of the *i.MX 8M Plus Applications Processor Reference Manual* illustrates the IOMUX scheme. "Table 8-1" of "Section 8" in that document also describes which i.MX 8M Plus pads correspond to which GPIO using alternate mode 5 or ALT5. The application design needs to keep in mind which pads have been assigned as a dedicated interface on the SOM as well as on the baseboard.

The *i.MX 8M Plus Applications Processor Reference Manual* also provides a table of associated control, mask, and status registers for each group of GPIO interrupts. Each interrupt can be configured as level or edge on an individual basis.

10.4 JTAG Debug Interface

The i.MX 8M Plus SOM routes the JTAG interface to the host off-board connectors. These signals are routed to a JTAG header (J29) on the baseboard. See Figure 1 for a picture which includes the J29 JTAG header, between the SOM connector and the J33 header. The pin mapping for the 10-pin (2x5) JTAG header is shown in the table below.

Pin #	Signal Name	Function	I/O	Voltage Ref	Reference Voltage Domain
1	1.8V (100-ohm PU)	JTAG Power	PWR	1.8V	1V8_IN
2	JTAG_TMS	JTAG_TMS	I	1.8V	NVCC_1V8
3	DGND	Ground	PWR	GND	--
4	JTAG_TCK	JTAG_TCK	I	1.8V	NVCC_1V8
5	DGND	Ground	PWR	GND	--
6	JTAG_TDO	JTAG_TDO	O	1.8V	NVCC_1V8
7	No Connect (default)	No Connect (default) or Ground when R448 installed	--	--	--
8	JTAG_TDI	JTAG_TDI	I	1.8V	NVCC_1V8
9	DGND	Ground	PWR	GND	--
10	nPOR	nPOR	O	1.8V	NVCC_SNVS_1P8

Table 28: JTAG Connector (J29) Pin Mapping

10.5 Power Supplies

10.5.1 Baseboard Power Supply Structure

The entire i.MX 8M Plus Development Kit is powered from a single connector (J38) on the baseboard. Users must use a USB-C power supply with the minimum voltage range of +5 to +20V (recommend a minimum of +9V) like the one provided originally with the development kit (Qualtek FWC-45-20-USCR). The USB-C cable is used to connect the USB-C power supply to the USB-C connector on the baseboard at J38. See Figure ***1***: Baseboard (Front Side) for a picture which includes the USB-C power-in jack (J38) flagged on the lower right side. Just below the power connectors is the Main Power On-Off Switch (S6).

A block diagram of the baseboard power structure is shown in the figure below.

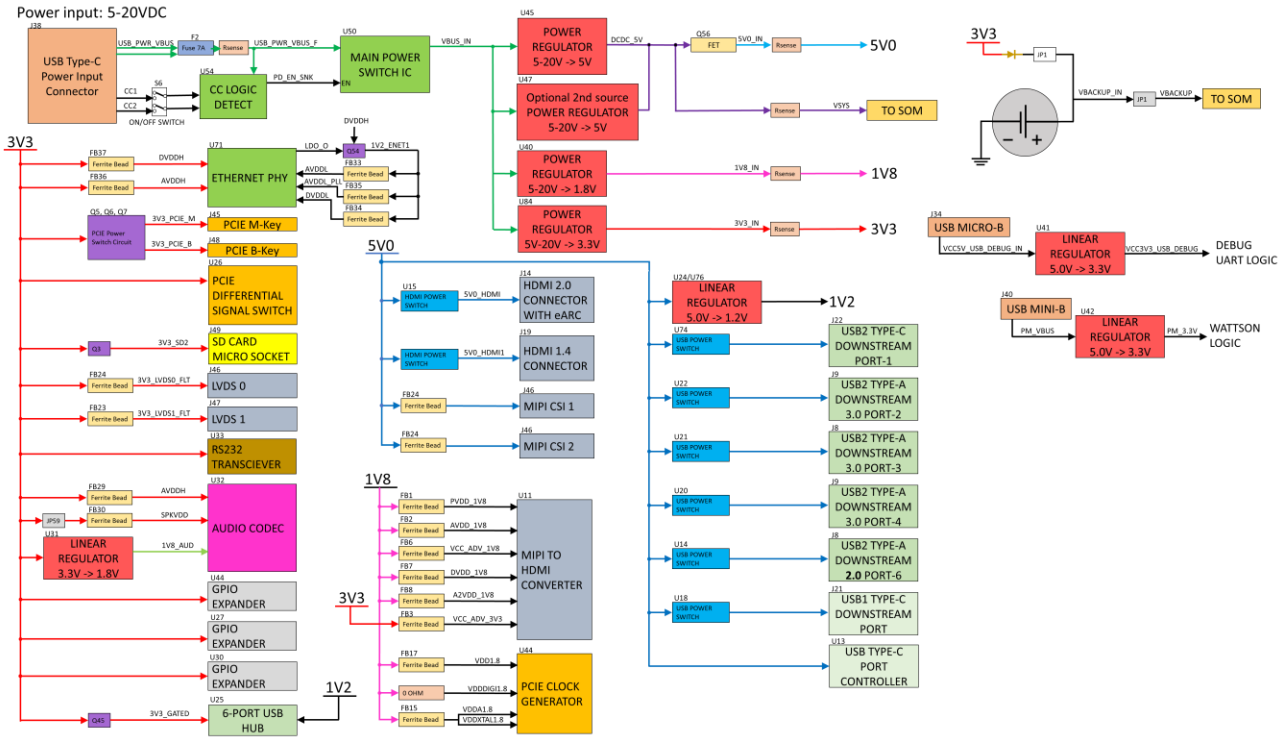

Figure 16: Baseboard Power Structure Block Diagram

10.5.1.1 USB_PWR_VBUS (+5V to +20V)

The i.MX 8M Plus baseboard supplies power to the SOM from the USB_PWR_VBUS supply connecting to the USB-C connector J38. This supply is monitored by Wattson and listed as “Kit: System Power.” The USB_PWR_VBUS power can be measured with Wattson using the power monitor 5 through R586.

The recommendation is to run at 9V or higher since the output of U45 is 5V.

10.5.1.1.1 DCDC_5V/VSYS

The USB_PWR_VBUS supply is regulated by the Monolithic Power Systems MP8759GD-Z synchronous step-down regulator (U45) and output signals is DCDC_5V.

DCDC_5V is the source supply for the VSYS voltage domain on the baseboard through R262. The VSYS supply is always enabled when USB_PWR_VBUS is active and S6 switch is turned on. This supply is the primary supply used to power the SOM. VSYS can be accessed on the baseboard at locations JP5 (pins 1 and 2) or J39 (pin 6). VSYS power can be measured with Wattson using power monitor 1 through R262.

The i.MX 8M Plus SOM receives VSYS (+5.0V) from the baseboard via the host connector. See the details of the SOM power supplies in the i.MX8M Plus Hardware Specification.

(i) 5V0

The 5V0 supply is powered directly from DCDC_5V through a FET Q56 and enabled when NVCC_3V3 is present. The 5V0 is used to power HDMI 2.0 connector with eARC, HDMI 1.4 connector, Camera, and USB interfaces. 5V0 can be accessed on the baseboard at locations JP4 (pins 1 and 2) and J39 (pin 8). The 5V0 power can be measured with Wattson using power monitor 2 through R577.

1. 1V2

The 1V2 supply is sourced by the 5V0 supply. There exist two possible 1.2V regulators. One labeled as the 1.2V regular in the schematics as using the Microchip Technology MIC23201YML switching voltage regulator (U24) and the other labeled as the alternate 1.2V regulator using the Texas Instruments TPS54612PWP synchronous buck PWM switcher with integrated FETs (U76). The default populated option is the TI U76 option. The PG_1V2 is used as a power good signal to both regulator options.

The 1V2 cannot be easily accessed through a header on the baseboard. The 1V2 voltage domain is not monitory by Wattson.

10.5.1.1.2 3V3

The 3V3 supply is regulated by the Analog Devices LT8610 synchronous step-down regulator (U84). VBUS_IN is the input supply for the 3V3 regulator. 3V3 can be accessed on the baseboard at locations J41 (pins 1 and 2), and J39 (pin 10). The 3V3 power can be measured with Wattson using power monitor 6 through power measurement resistor R329. This supply is the primary supply used on the baseboard for 3.3V but is also used as an optional VBACKUP_IN source through JP1 and used to provide 3.3V to the MIPI to HDMI converter through a ferrite bead (FB3).

(i) 3v3_GATED

The 3V3_GATED supply is powered by the 3V3 domain through a P-CH FET (Q55). This FET is enabled using the PG_1V2 signal through an N-CH FET. The 3V3_GATED domain is not separately monitored by Wattson and is not accessible through a dedicated pin on a baseboard header.

10.5.1.1.3 1V8

The 1V8 supply is regulated by the Analog Devices LT8610A synchronous step-down regulator (U40). VBUS_IN is the input supply for the 1V8 regulator. This supply is monitor by Wattson as monitor 4. The 1V8 power can be accessed on the baseboard at locations J36 (pins 1 and 2), and J39 (pin 2).

10.5.2 VBACKUP

The baseboard provides a VBACKUP rail to power the PCF85263ATT RTC on the SOM when VSYS is not present. VBACKUP is derived from a coin cell battery (3.0V) on the baseboard. The VBACKUP power can be measured with Wattson using power monitor 3 through power measurement resistor R588. The VBACKUP domain can be accessed on the baseboard at location J25 (pin 1).

Alternatively, VBACKUP can be powered and charged by 3V3 if jumper JP1 is installed.

11 Electrical Specification

11.1 Absolute Maximum Ratings

The i.MX 8M Plus Development Kit absolute maximum specifications are shown in the table below.

Parameter	Symbol	Min (V)	Max (V)
DC Main System External Supply	J38	VSS-0.3	20
RTC Backup Battery Voltage	VBACKUP_IN	VSS-0.3	3.3

Table 29: Absolute Maximum Ratings

NOTE: These stress ratings are only for transient conditions. Operation at or beyond absolute maximum rating conditions may affect reliability and cause permanent damage to the i.MX 8M Plus SOM and baseboard.

11.2 Recommended Operating Conditions

The i.MX 8M Plus Development Kit temperature specifications are shown in the table below.

Parameter	Symbol	Min (V)	Typ (V)	Max (V)	Units
DC Main System External Supply	J38	5.0	9.0	20	V
RTC Backup Battery Voltage	VBACKUP_IN	0.9[8]	3.0	3.3	V
Operating Temperature	--	0	--	70	°C
Storage Temperature	--	0	--	70	°C

Table 30: Recommended Operating Conditions

[8] For reliable oscillator start-up at power-on use VBACKUP_IN (PCF85263A.VDD) greater than 1.2 V. If powered up at 0.9 V the oscillator will start but it might be a bit slow, especially if at high temperature. Normally the power supply is not 0.9 V at start-up and only comes at the end of battery discharge. VDD min of 0.9 V is specified so that the customer can calculate how large a battery or capacitor they need for their application. VDD min of 1.2 V or greater is needed to ensure speedy oscillator start-up time. The RTC was tested by NXP at 1.8V for 400 KHz I2C operation.

12 Environment

12.1 ESD Considerations

The i.MX 8M Plus SOM extends and integrates with the baseboard functionality and was not designed to be hot-plugged or have external ports exposed to direct end user access. The i.MX 8M Plus SOMs are static sensitive devices. Care should be taken when handling to avoid contact with charged persons, devices, or surfaces.

The i.MX 8M Plus SOM does not incorporate any ESD protection and therefore, relies on the baseboard to provide the protection at the point of contact for any externally accessible connectors or access points that directly route to the SOM.

13 Baseboard Connectors - Pin Descriptions & Functions

The tables in this section describe the signals as seen on the connectors on the baseboard that interface to the Beacon EmbeddedWorks SOMs.

13.1 J1 Baseboard Connector

J1 Pin#	Signal Name	BGA Ball#	Processor Signal	Processor Alternate Functions	I/O	Voltage (V)	Signal Description
J1.1	VSYS	---	---	---	PWR	3.825-5.5	Main SOM power input rail.
J1.2	VSYS	---	---	---	PWR	3.825-5.5	Main SOM power input rail.
J1.3	VSYS	---	---	---	PWR	3.825-5.5	Main SOM power input rail.
J1.4	VSYS	---	---	---	PWR	3.825-5.5	Main SOM power input rail.
J1.5	VSYS	---	---	---	PWR	3.825-5.5	Main SOM power input rail.
J1.6	VSYS	---	---	---	PWR	3.825-5.5	Main SOM power input rail.
J1.7	VSYS	---	---	---	PWR	3.825-5.5	Main SOM power input rail.
J1.8	VSYS	---	---	---	PWR	3.825-5.5	Main SOM power input rail.
J1.9	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J1.10	VSYS	---	---	---	PWR	3.825-5.5	Main SOM power input rail.
J1.11	N29246748 (LDO5)	---	---	---	PWR	0.8 to 3.3	User configurable LDO from the PMIC. Off by default. Please see the *PCA9450C PMIC Datasheet* for more information. R369 not populated by default.
J1.12	VSYS	---	---	---	PWR	3.825-5.5	Main SOM power input rail.
J1.13	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J1.14	VSYS	---	---	---	PWR	3.825-5.5	Main SOM power input rail.
J1.15	N29246763 (NVCC_DRAM_1V1)	---	---	---	---	---	Test Only. Do not connect. R368 not populated by default.
J1.16	VSYS	---	---	---	PWR	3.825-5.5	Main SOM power input rail.
J1.17	NVCC_1V8	---	---	---	PWR	1.8	1.8V power rail. May be used for reference voltage on user designs.
J1.18	VSYS	---	---	---	PWR	3.825-5.5	Main SOM power input rail.
J1.19	NVCC_3V3	---	---	---	PWR	3.3	3.3V power rail. May be used for reference voltage on user designs.

J1 Pin#	Signal Name	BGA Ball#	Processor Signal	Processor Alternate Functions	I/O	Voltage (V)	Signal Description
J1.20	VSYS	---	---	---	PWR	3.825-5.5	Main SOM power input rail.
J1.21	N29246825 (VDDA_1V8)	---	---	---	---	---	Test Only. Do not connect. R367 not populated by default.
J1.22	VSYS	---	---	---	PWR	3.825-5.5	Main SOM power input rail.
J1.23	N29246866 (32KOUT)	---	---	---	I	1.8	Clock output from PCF85263A RTC. Can be programmed by software. R370 populated by default.
J1.24	VSYS	---	---	---	PWR	3.825-5.5	Main SOM power input rail.
J1.25	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J1.26	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J1.27	CLKOUT1	K29	CLKOUT1		I	1.8	Clock Out 1
J1.28	CLKIN1	K28	CLKIN1		O	1.8	Clock In 1
J1.29	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J1.30	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J1.31	CLKOUT2	L29	CLKOUT2		I	1.8	Clock Out 2
J1.32	SD2_nCD	AD29	SD2_CD_B	USDHC2_CD_B, GPIO2_IO12	O	1.8/3.3	uSDHC2 Card detection pin
J1.33	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J1.34	LVDS0_CLK_N	G28	LVDS0_CLK_N	---	I	See Note 1	LVDS0 CLK N. Route as 100-ohm differential pair with LVDS0_CLK_P.
J1.35	CLKIN2	L28	CLKIN2		O	1.8	Clock In 2
J1.36	LVDS0_CLK_P	F29	LVDS0_CLK_P	---	I	See Note 1	LVDS0 CLK P. Route as 100-ohm differential pair with LVDS0_CLK_N.
J1.37	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J1.38	LVDS0_D0_N	E28	LVDS0_D0_N	---	I	See Note 1	LVDS0 Data0 N. Route as 100-ohm differential pair with LVDS0_D0_P.
J1.39	LVDS0_D1_N	F28	LVDS0_D1_N	---	I	See Note 1	LVDS0 Data1 N. Route as 100-ohm differential pair with LVDS0_D1_P.
J1.40	LVDS0_D0_P	D29	LVDS0_D0_P	---	I	See Note 1	LVDS0 Data0 P. Route as 100-ohm differential pair with LVDS0_D0_N.
J1.41	LVDS0_D1_P	E29	LVDS0_D1_P	---	I	See Note 1	LVDS0 Data1 P. Route as 100-ohm differential pair with LVDS0_D0_N.
J1.42	DGND	---	---	---	---	GND	Ground. Connect to digital ground.

J1 Pin#	Signal Name	BGA Ball#	Processor Signal	Processor Alternate Functions	I/O	Voltage (V)	Signal Description
J1.43	ENET1_TXC_R	AH14	SAI1_TXD5	SAI1_TX_DATA05, SAI6_RX_DATA00, SAI6_TX_DATA00, ENET1_RGMII_TXC, GPIO4_IO17	I	1.8	Ethernet Interface 1 RGMII Transmit Clock.
J1.44	ENET1_NRST	AC12	SAI1_TXD6	SAI1_TX_DATA06, SAI6_RX_SYNC, SAI6_TX_SYNC, ENET1_RX_ER, GPIO4_IO18	I	1.8	Ethernet 1 Reset.
J1.45	ENET1_TD3_R	AD12	SAI1_TXD3	SAI1_TX_DATA03, ENET1_RGMII_TD3, GPIO4_IO15	I	1.8	Ethernet Interface 1 RGMII Transmit Data 3.
J1.46	TCPC_NINT1	AJ13	SAI1_TXD7	SAI1_TX_DATA07, SAI6_MCLK, PDM_CLK, ENET1_TX_ER, GPIO4_IO19	I	1.8	Type-C Port Controller Interrupt.
J1.47	SYS_nRST	---	---	---	O, OD	1.8	System Reset. This is the main reset for the SOM. It resets the PMIC and Processor. This signal has a pull-up internal to the PMIC.
J1.48	ENET1_TD2_R	AH11	SAI1_TXD2	SAI1_TX_DATA02, ENET1_RGMII_TD2, GPIO4_IO14	I	1.8	Ethernet Interface 1 RGMII Transmit Data 2.
J1.49	ENET1_TD0_R	AJ11	SAI1_TXD0	SAI1_TX_DATA00, ENET1_RGMII_TD, GPIO4_IO12	I	1.8	Ethernet Interface 1 RGMII Transmit Data 0.
J1.50	ENET1_TD1_R	AJ10	SAI1_TXD1	SAI1_TX_DATA01, ENET1_RGMII_TD1, GPIO4_IO13	I	1.8	Ethernet Interface 1 RGMII Transmit Data 1.
J1.51	nPOR	J29	POR_B		O, OD	1.8	Power-On Reset. This is an output of the PMIC to hold the processor in reset. SYS_nRST is the main reset that should be used on the baseboard. This signal has a 100k ohm pull-up.
J1.52	ENET1_TX_CTL_R	AH13	SAI1_TXD4	SAI1_TX_DATA04, SAI6_RX_BCLK, SAI6_TX_BCLK, ENET1_RGMII_TX_CTL, GPIO4_IO16	I	1.8	Ethernet Interface 1 RGMII Transmit Control.
J1.53	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J1.54	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J1.55	GPIO2_IO11	W26	SD1_STROBE	USDHC1_STROBE, GPIO2_IO11	I/O	1.8	This signal may be used as a GPIO.
J1.56	ENET1_RD2	AH10	SAI1_RXD6	SAI1_RX_DATA06, SAI6_TX_SYNC, SAI6_RX_SYNC, ENET1_RGMII_RD2, GPIO4_IO08	O	1.8	Ethernet Interface 1 RGMII Receive Data 2.
J1.57	ENET1_RD3	AH12	SAI1_RXD7	SAI1_RX_DATA07, SAI6_MCLK, SAI1_TX_SYNC, SAI1_TX_DATA04, ENET1_RGMII_RD3, GPIO4_IO09	O	1.8	Ethernet Interface 1 RGMII Receive Data 3.
J1.58	ENET1_RD1	AE10	SAI1_RXD5	SAI1_RX_DATA05, SAI6_TX_DATA00, SAI6_RX_DATA00, SAI1_RX_SYNC, ENET1_RGMII_RD1, GPIO4_IO07	O	1.8	Ethernet Interface 1 RGMII Receive Data 1.
J1.59	ENET1_RD0	AD10	SAI1_RXD4	SAI1_RX_DATA04, SAI6_TX_BCLK, SAI6_RX_BCLK, ENET1_RGMII_RD0, GPIO4_IO06	O	1.8	Ethernet Interface 1 RGMII Receive Data 0.
J1.60	ENET1_MDC	AH9	SAI1_RXD2	SAI1_RX_DATA02, SAI5_RX_DATA02, AUDIOMIX_PDM_BIT_STREAM02, ENET1_MDC, GPIO4_IO04	O	1.8	Ethernet Interface 1 RGMII Management Data Clock.

J1 Pin#	Signal Name	BGA Ball#	Processor Signal	Processor Alternate Functions	I/O	Voltage (V)	Signal Description
J1.61	ENET1_MDIO	AJ8	SAI1_RXD3	SAI1_RX_DATA03, PDM_BIT_STREAM03, SAI1_RXD3__ENET1_MDIO, GPIO4_IO05	O	1.8	Ethernet Interface 1 RGMII Management Data Input/Output.
J1.62	ENET1_RX_CTL	AF12	SAI1_TXFS	SAI1_TX_SYNC, ENET1_RGMII_RX_CTL, GPIO4_IO10	I	1.8	Ethernet Interface 1 RGMII Receive Control.
J1.63	SAI2_RXFS	AH17	SAI2_RXFS	SAI2_RX_SYNC, SAI5_TX_SYNC, SAI5_TX_DATA01, SAI2_RX_DATA01, UART1_DCE_TX, UART1_DTE_RX, PDM_BIT_STREAM02, GPIO4_IO21	O	1.8	Synchronous Audio Interface 2 Receive Frame Sync
J1.64	SAI2_MCLK	AJ15	SAI2_MCLK	SAI2_MCLK, SAI3_MCLK , SAI5_MCLK, ENET_QOS_1588_EVENT3_IN, CAN2_RX, ENET_QOS_1588_EVENT3_AUX_IN, GPIO4_IO27	I	1.8	Synchronous Audio Interface 2 Master Clock
J1.65	TPM_RST_N	AJ9	SAI1_RXFS	SAI1_RX_SYNC, ENET1_1588_EVENT0_IN, GPIO4_IO00	O	1.8	Trusted Platform Module Reset.
J1.66	SAI1_RXC	AH8	SAI1_RXC	SAI1_RX_BCLK, PDM_CLK, ENET1_1588_EVENT0_OUT, GPIO4_IO01	O	1.8	Synchronous Audio Interface 1 Receive Bit Clock.
J1.67	LVDS0_D2_N	H28	LVDS0_D2_N	---	I	See Note 1	LVDS0 Data2 N. Route as 100-ohm differential pair with LVDS0_D2_P.
J1.68	N29222252 (VDD_SOC)	---	---	---	---	---	Test Only. Do not connect. R443 not populated by default.
J1.69	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J1.70	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J1.71	LVDS0_D2_P	G29	LVDS0_D2_P	---	I	See Note 1	LVDS0 Data2 P. Route as 100-ohm differential pair with LVDS0_D2_N.
J1.72	SAI5_RXD0	AE16	SAI5_RXD0	SAI5_RX_DATA00, SAI1_TX_DATA02, PWM2_OUT, I2C5_SCL, PDM_BIT_SREAM00, GPIO3_IO21	O	1.8	Synchronous Audio Interface 5 Receive Data 0
J1.73	SAI1_TXC	AJ12	SAI1_TXC	SAI1_TX_BCLK, SAI5_TX_BCLK, ENET1_RGMII_RXC, GPIO4_IO11	I	1.8	Ethernet Interface 1 RGMII Receive Clock.
J1.74	GPIO1_IO06	A3	GPIO1_IO06	GPIO1_IO06, ENET_QOS_MDC, ISP_SHUTTER_TRIG_1, USDHC1_CD_B, CCM_EXT_CLK3	I/O	1.8	This signal may be used as a GPIO.
J1.75	SAI5_RXC	AD14	SAI5_RXC	SAI5_RX_BCLK, SAI1_TX_DATA01, PWM3_OUT, I2C6_SDA, PDM_CLK, GPIO3_IO20	O	1.8	Synchronous Audio Interface 5 Receive Bit Clock
J1.76	GPIO1_IO07	F6	GPIO1_IO07	GPIO1_IO07, ENET_QOS_MDIO, USDHC1_WP, ISP_FLASH_TRIG_1, CCM_EXT_CLK4	I/O	1.8	This signal may be used as a GPIO.
J1.77	GPIO1_IO05	B4	GPIO1_IO05	GPIO1_IO05, M7_NMI, ISP_FL_TRIG_1, CCM_PMIC_READY	I/O	1.8	This signal may be used as a GPIO.
J1.78	SAI1_MCLK	AE12	SAI1_MCLK	SAI1_MCLK, SAI5_MCLK, SAI1_TX_BCLK, GPIO4_IO20	I	1.8	Synchronous Audio Interface 1 Master Clock

J1 Pin#	Signal Name	BGA Ball#	Processor Signal	Processor Alternate Functions	I/O	Voltage (V)	Signal Description
J1.79	SAI5_MCLK	AF14	SAI5_MCLK	SAI5_MCLK, SAI1_TX_BCLK, PWM1_OUT, I2C5_SDA, CAN2_RX, GPIO3_IO25	I	1.8	Synchronous Audio Interface 5 Master Clock
J1.80	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J1.81	SAI5_RXD2	AF16	SAI5_RXD2	SAI5_RX_DATA02, SAI1_TX_DATA04, SAI1_TX_SYNC, SAI5_TX_BCLK, PDM_BIT_STREAM02, CAN1_RX, GPIO3_IO23	O	1.8	Synchronous Audio Interface 5 Receive Data 2
J1.82	LVDS0_D3_N	J28	LVDS0_D3_N	---	I	See Note 1	LVDS0 Data3 N. Route as 100-ohm differential pair with LVDS0_D3_P.
J1.83	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J1.84	LVDS0_D3_P	H29	LVDS0_D3_P	---	I	See Note 1	LVDS0 Data3 P. Route as 100-ohm differential pair with LVDS0_D3_N.
J1.85	SAI5_RXD3	AE14	SAI5_RXD3	SAI5_RX_DATA03, SAI1_TX_DATA05, SAI1_TX_SYNC, SAI5_TX_DATA00, PDM_BIT_STREAM03, CAN2_TX, GPIO3_IO24	O	1.8	Synchronous Audio Interface 5 Receive Data 3
J1.86	N29225112 (NVCC_SNVS_1V8)	---	---	---	---	---	Test Only. Do not connect. R442 not populated by default.
J1.87	RTC_nINTA	A6	GPIO1_IO13	GPIO1_IO13, USB1_OC, PWM2_OUT	I	1.8	RTC Interrupt output.
J1.88	VDD_MIPI_1P2_CAP	---	---	---	---	---	Test Only. Do not connect.
J1.89	I2C4_SCL	AF8	I2C4_SCL	I2C4_SCL, PWM2_OUT, PCIE_CLKREQ_B, ECSPI2_MISO, GPIO5_IO20	I/O, OD	1.8	I2C4 Clock. This signal has a 4.7k ohm pull-up.
J1.90	N29225121 (VDD_ARM)	---	---	---	---	---	Test Only. Do not connect. R441 not populated by default.
J1.91	I2C4_SDA	AD8	I2C4_SDA	I2C4_SDA, PWM1_OUT, ECSPI2_SS0, GPIO5_IO21	I/O, OD	1.8	I2C4 Data. This signal has a 4.7k ohm pull-up.
J1.92	SAI5_RXD1	AD16	SAI5_RXD1	SAI5_RX_DATA01, SAI1_TX_DATA03, SAI1_TX_SYNC, SAI5_TX_SYNC, PDM_BIT_STREAM01 , CAN1_TX, GPIO3_IO22	O	1.8	Synchronous Audio Interface 5 Receive Data 1
J1.93	ONOFF	G22	ONOFF	SNVS_ONOFF	O	1.8	Interrupt or power sequence signal. Please see Section 5.2.2 and the *i.MX 8M Plus Reference Manual* for more information. This signal has a 100k ohm pull-up.
J1.94	SAI5_RXFS	AC14	SAI5_RXFS	SAI5_RX_SYNC, SAI1_TX_DATA00, PWM4_OUT, I2C6_SCL, GPIO3_IO19	O	1.8	Synchronous Audio Interface 5 Receive Frame Sync.
J1.95	I2C3_SDA	AJ6	I2C3_SDA	I2C3_SDA, PWM3_OUT, GPT3_CLK, ECSPI2_MOSI, GPIO5_IO19	I/O, OD	1.8	I2C3 Data. This signal has a 4.7k ohm pull-up.

J1 Pin#	Signal Name	BGA Ball#	Processor Signal	Processor Alternate Functions	I/O	Voltage (V)	Signal Description
J1.96	N29225140 (VDD_SNVS_0V8)	---	---	---	---	---	Test Only. Do not connect. R440 not populated by default.
J1.97	I2C3_SCL	AJ7	I2C3_SCL	I2C3_SCL, PWM4_OUT, GPT2_CLK, ECSPI2_SCLK, GPIO5_IO18	I/O, OD	1.8	I2C3 Clock. This signal has a 4.7k ohm pull-up.
J1.98	SAI3_MCLK	AJ20	SAI3_MCLK	SAI3_MCLK, PWM4_OUT, SAI5_MCLK, SPDIF1_OUT, SPDIF1_IN, GPIO5_IO02	I	1.8	Synchronous Audio Interface 3 Master Clock
J1.99	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J1.100	DGND	---	---	---	---	GND	Ground. Connect to digital ground.

Table 31: J1 Baseboard Connector Pin Mapping

TABLE NOTES:

1. LVDS voltage levels follow the LVDS specification. Please see TIA/EIA STANDARD 644-A standard for more information.

13.2 J2 Baseboard Connector

J2 Pin#	Signal Name	BGA Ball#	Processor Signal	Processor Alternate Functions	I/O	Voltage (V)	Description
J2.1	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J2.2	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J2.3	SD2_CLK	AB29	SD2_CLK	USDHC2_CLK, GPIO2_IO13	I	1.8/3.3	uSDHC2 Clock. R627 not populated by default.
J2.4	N29227931 (NVCC_SD2)		---	---	PWR	1.8/3.3	uSDHC2 Power, 1.8V if SD2_VSEL is high and 3.3 if SD2_VSEL is low. R125 not populated by default.
J2.5	SD2_CMD	AB28	SD2_CMD	USDHC2_CMD, GPIO2_IO14	I	1.8/3.3	uSDHC2 Command Line
J2.6	N28370290 (MIPI_CSI2_CLK_N)	B23	MIPI_CSI2_CLK_N	---	O	See Note 1	MIPI CSI-2 Clock N. Route as 100-ohm differential pair with CSI2_CKP. R123 not populated by default.
J2.7	SD2_DAT0	AC28	SD2_DATA0	USDHC2_DATA0, GPIO2_IO15	I/O	1.8/3.3	uSDHC2 Data 0
J2.8	N28370297 (MIPI_CSI2_CLK_P)	A23	MIPI_CSI2_CLK_P	---	O	See Note 1	MIPI CSI-2 Clock P. Route as 100-ohm differential pair with CSI2_CKN. R122 not populated by default.
J2.9	SD2_DAT1	AC29	SD2_DATA1	USDHC2_DATA1, GPIO2_IO16	I/O	1.8/3.3	uSDHC2 Data 1
J2.10	N28370304 (MIPI_CSI2_D0_N)	B25	MIPI_CSI2_D0_N	---	O	See Note 1	MIPI CSI-2 Data 0 N. Route as 100-ohm differential pair with CSI2_DN0. R119 not populated by default.
J2.11	SD2_DAT2	AA26	SD2_DATA2	USDHC2_DATA2, GPIO2_IO17	I/O	1.8/3.3	uSDHC2 Data 2
J2.12	N28370311 (MIPI_CSI2_D0_P)	A25	MIPI_CSI2_D0_P	---	O	See Note 1	MIPI CSI-2 Data 0 P. Route as 100-ohm differential pair with CSI2_DP0. R118 not populated by default.
J2.13	SD2_DAT3	AA25	SD2_DATA3	USDHC2_DATA3, GPIO2_IO18	I/O	1.8/3.3	uSDHC2 Data 3
J2.14	N28370318 (MIPI_CSI2_D1_N)	B24	MIPI_CSI2_D1_N	---	O	See Note 1	MIPI CSI-2 Data 1 N. Route as 100-ohm differential pair with CSI2_DN1. R117 not populated by default.
J2.15	SD2_WP	AC26	SD2_WP	USDHC2_WP, GPIO2_IO20	O	1.8/3.3	USB Interface 1 Type C Enable. L = Normal operation, H = Shutdown
J2.16	N28370325 (MIPI_CSI2_D1_P)	A24	MIPI_CSI2_D1_P	---	O	See Note 1	MIPI CSI-2 Data 1 P. Route as 100-ohm differential pair with CSI2_DP1. R116 not populated by default.
J2.17	SD2_nRST	AD28	SD2_RESET_B	USDHC2_RESET_B, GPIO2_IO19	I	1.8/3.3	uSDHC2 Reset. This signal has a 4.7k ohm pull-up.

J2 Pin#	Signal Name	BGA Ball#	Processor Signal	Processor Alternate Functions	I/O	Voltage (V)	Description
J2.18	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J2.19	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J2.20	PMIC_nINT	D6	GPIO1_IO03	GPIO1_IO03, USDHC1_VSELECT, ISP_PRELIGHT_TRIG_0, SDMA1_EXT_EVENT00	I/O, OD	1.8	The primary use is an interrupt output from the PMIC to the processor. This signal could also be used as a shared open drain input/interrupt to the processor through the host connector. The processor internal pull-up is enabled for this signal.
J2.21	N29242105 (MIPI_CSI2_D3_N)	B21	MIPI_CSI2_D3_N	---	O	See Note 1	MIPI CSI-2 Data 3 N. Route as 100-ohm differential pair with CSI2_DP3. R110 not populated by default.
J2.22	PMIC_STBY_REQ	J24	PMIC_STBY_REQ	CCM_PMIC_STBY_REQ	I	1.8	Used by the processor to tell the PMIC to go into Standby mode.
J2.23	N29242108 (MIPI_CSI2_D3_P)	A21	MIPI_CSI2_D3_P	---	O	See Note 1	MIPI CSI-2 Data 3 P. Route as 100-ohm differential pair with CSI2_DN3. R107 not populated by default.
J2.24	BOOT_MODE0	G10	BOOT_MODE0	SRC_BOOT_MODE0	O	1.8	Boot Mode 0 pin. See Section 5.1 for more information.
J2.25	HDMI_TX0_N	AJ25	HDMI_TX0_N		I	1.8	HDMI_TX0 N. Route as 100-ohm differential pair with HDMI_TX0_P.
J2.26	BOOT_MODE1	F8	BOOT_MODE1	SRC_BOOT_MODE1	O	1.8	Boot Mode 1 pin. See Section 5.1 for more information.
J2.27	HDMI_TX0_P	AH25	HDMI_TX0_P	---	I	1.8	HDMI_TX0 P. Route as 100-ohm differential pair with HDMI_TX0_N.
J2.28	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J2.29	HDMI_TXC_N	AJ24	HDMI_TXC_N	---	I	1.8	HDMI_TXC N. Route as 100-ohm differential pair with HDMI_TXC_P.
J2.30	HDMI_TX1_N	AJ26	HDMI_TX1_N	---	I	1.8	HDMI_TX1 N. Route as 100-ohm differential pair with HDMI_TX1_P.
J2.31	HDMI_TXC_P	AH24	HDMI_TXC_P	---	I	1.8	HDMI_TXC P. Route as 100-ohm differential pair with HDMI_TXC_N.
J2.32	HDMI_TX1_P	AH26	HDMI_TX1_P		I	1.8	HDMI_TX1 P. Route as 100-ohm differential pair with HDMI_TX1_N.
J2.33	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J2.34	HDMI_TX2_N	AJ27	HDMI_TX2_N	---	I	1.8	HDMI_TX2 N. Route as 100-ohm differential pair with HDMI_TX2_P.

J2 Pin#	Signal Name	BGA Ball#	Processor Signal	Processor Alternate Functions	I/O	Voltage (V)	Description
J2.35	HDMI_DDC_SCL	AC22	HDMI_DDC_SCL	---	I	1.8	HDMI DDC Clock
J2.36	HDMI_TX2_P	AH27	HDMI_TX2_P	---	I	1.8	HDMI_TX2 P. Route as 100-ohm differential pair with HDMI_TX2_N.
J2.37	HDMI_DDC_SDA	AF22	HDMI_DDC_SDA	---	I/O	1.8	HDMI DDC Data
J2.38	HDMI_CEC	AD22	HDMI_CEC	---	I/O	1.8	HDMI CEC (Consumer Electronics Control)
J2.39	---	---	---	---	---	---	Reserved for future use. Do not connect.
J2.40	HDMI_HPD	AE22	HDMI_HPD		O	1.8	HDMI Hot Plug Detection
J2.41	SAI1_RXD1	AF10	SAI1_RXD1	SAI1_RX_DATA01, PDM_BIT_STREAM01, ENET1_1588_EVENT1_OUT, GPIO4_IO03	O	1.8	Ethernet Interface 1 Interrupt. R532 not populated by default.
J2.42	SAI1_RXD0	AC10	SAI1_RXD0	SAI1_RX_DATA00, SAI1_TX_DATA00, PDM_BIT_STREAM00, ENET1_1588_EVENT1_IN, GPIO4_IO02	O	1.8	Ethernet Interface 1 Wake-On-LAN. R531 populated by default.
J2.43	GPIO1_IO01	E8	GPIO1_IO01	GPIO1_IO01, PWM1_OUT, ISP_SHUTTER_TRIG_0, REF_CLK_24M, CCM_EXT_CLK2	I/O	1.8	This signal may be used as a GPIO.
J2.44	GPIO1_IO09	B8	GPIO1_IO09	GPIO1_IO09, ENET_QOS_1588_EVENT0_OUT, PWM2_OUT, ISP_SHUTTER_OPEN_1, USDHC3_RESET_B, SDMA2_EXT_EVENT00	I/O	1.8	This signal may be used as a GPIO.
J2.45	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J2.46	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J2.47	---	---	---	---	---	---	Reserved for future use. Do not connect.
J2.48	GPIO1_IO08	A8	GPIO1_IO08	GPIO1_IO08, ENET_QOS_1588_EVENT0_IN, PWM1_OUT, ISP_PRELIGHT_TRIG_1, ENET_QOS_1588_EVENT0_AUX_IN, USDHC2_RESET_B	I/O	1.8	This signal may be used as a GPIO.
J2.49	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J2.50	SPDIF_TX	AE18	SPDIF_TX	SPDIF1_OUT, PWM3_OUT, I2C5_SCL, GPT1_COMPARE1, CAN1_TX, GPIO5_IO03	I	1.8	Sony/Philips Digital Interface Transmit Data
J2.51	---	---	---	---	---	---	Reserved for future use. Do not connect.
J2.52	SPDIF_RX	AD18	SPDIF_RX	SPDIF1_IN, PWM2_OUT, I2C5_SDA, CAN1_RX, GPIO5_IO04	O	1.8	Sony/Philips Digital Interface Receive Data
J2.53	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J2.54	SPDIF_EXT_CLK	AC18	SPDIF_EXT_CLK	SPDIF1_EXT_CLK, PWM1_OUT, GPT1_COMPARE3, GPIO5_IO05	I	1.8	Sony/Philips Digital Interface External Clock

J2 Pin#	Signal Name	BGA Ball#	Processor Signal	Processor Alternate Functions	I/O	Voltage (V)	Description
J2.55	SAI3_RXFS	AJ19	SAI3_RXFS	SAI3_RX_SYNC, SAI2_RX_DATA01, SAI5_RX_SYNC, SAI3_RX_DATA01, PDM_BIT_STREAM00, SPDIF1_IN, GPIO4_IO28	O	1.8	Synchronous Audio Interface 3 Receive Frame Sync
J2.56	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J2.57	SAI3_RXC	AJ18	SAI3_RXC	SAI3_RX_BCLK, SAI2_RX_DATA02, SAI5_RX_BCLK, GPT1_CLK, PDM_CLK, UART2_DCE_CTS, UART2_DTE_RTS, GPIO4_IO29	O	1.8	Trusted Platform Module Interrupt Request.
J2.58	SAI3_RXD	AF18	SAI3_RXD	SAI3_RX_DATA00, SAI2_RX_DATA03, SAI5_RX_DATA00, PDM_BIT_STREAM01, UART2_DCE_RTS, UART2_DTE_CTS, GPIO4_IO30	O	1.8	Synchronous Audio Interface 3 Receive Data
J2.59	SAI3_TXC	AH19	SAI3_TXC	SAI3_TX_BCLK, SAI2_TX_DATA02, SAI5_RX_DATA02, GPT1_CAPTURE1, UART2_DCE_TX, UART2_DTE_RX, PDM_BIT_STREAM02, GPIO5_IO00	I	1.8	Synchronous Audio Interface 3 Transmit Clock
J2.60	SAI3_TXD	AH18	SAI3_TXD	SAI3_TX_DATA00, SAI2_TX_DATA03, SAI5_RX_DATA03, GPT1_COMPARE2, GPIO5_IO01	I	1.8	Synchronous Audio Interface 3 Transmit Data
J2.61	GPIO1_IO12	A5	GPIO1_IO12	GPIO1_IO12, USB1 _PWR, SDMA2_EXT_EVENT01	I/O	1.8	Default: Reserved for future use. Do not connect. R83 populated: This signal may be used as a GPIO.
J2.62	EARC_P_UTIL	AJ23	EARC_P_UTIL	---	I/O	1.8	EARC P/UTIL
J2.63	EARC_AUX	AH23	EARC_AUX	---	O	1.8	EARC AUX
J2.64	EARC_N_HPD	AH22	EARC_N_HPD	---	I/O	1.8	EARC N/Hot Plug Detect
J2.65	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J2.66	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J2.67	LED_ACT	---	---	---	I	1.8	LED input for 10/100/1000 BASE-T activity. Active high. This signal has a 10k ohm pull-up. Note: This is a 1.8V signal and requires an external 3.3V to drive an LED.
J2.68	---	---	---	---	---	---	Reserved for future use. Do not connect.
J2.69	MIPI_CSI2_D2_N	B22	MIPI_CSI2_D2_N	---	O	See Note 1	MIPI CSI-2 Data 2 N. Route as 100-ohm differential pair with CSI2_DP2.
J2.70	LED_LINK	---	---	---	I	1.8	LED input for link. Active high. This signal has a 10k ohm pull-up. Note: This is a 1.8V signal and requires an external 3.3V to drive an LED.

J2 Pin#	Signal Name	BGA Ball#	Processor Signal	Processor Alternate Functions	I/O	Voltage (V)	Description
J2.71	MIPI_CSI2_D2_P	A22	MIPI_CSI2_D2_P	---	O	See Note 1	MIPI CSI-2 Data 2 P. Route as 100-ohm differential pair with CSI2_DN2.
J2.72	GPIO1_IO11	D8	GPIO1_IO11	GPIO1_IO11, USB2_ID, PWM2_OUT, USDHC3_VSELECT, CCM_PMIC_READY	I/O	1.8	This signal may be used as a GPIO.
J2.73	N30135192 (UART1_TXD)	AJ3	UART1_TXD	UART1_DCE_TX, UART1_DTE_RX, ECSPI3_MOSI, GPIO5_IO23	I/O	1.8	UART1 Transmit. R578 not populated by default.
J2.74	SAI3_TXFS	AC16	SAI3_TXFS	SAI3_TX_SYNC, SAI2_TX_DATA01, SAI5_RX_DATA01, SAI3_TX_DATA01, UART2_DCE_RX, UART2_DTE_TX, PDM_BIT_STREAM03, GPIO4_IO31	I	1.8	Synchronous Audio Interface 3 Transmit Frame Sync
J2.75	N30135195 (UART1_RXD)	AD6	UART1_RXD	UART1_DCE_RX, UART1_DTE_TX, ECSPI3_SCLK, GPIO5_IO22	O	1.8	UART1 Receive. R579 not populated by default.
J2.76	GPIO1_IO14	A4	GPIO1_IO14	GPIO1_IO14, USB2_PWR, USDHC3_CD_B, PWM3_OUT, CCM_CLKO1	I/O	1.8	This signal may be used as a GPIO.
J2.77	GPIO1_IO15	B5	GPIO1_IO15	GPIO1_IO15, USB2_OC, USDHC3_WP, PWM4_OUT, CCM_CLKO2	I/O	1.8	This signal may be used as a GPIO.
J2.78	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J2.79	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J2.80	ETH_TRX3_N	---	---	---	IA/OA	Variable (See Note 2)	Ethernet Media Dependent Interface[3]. Route as 100-ohm differential pair with ENET_TRX3_P. Requires external magnetics.
J2.81	ENET_XTLI	---	---	---	IA	1.2	Default this signal is not used. Could be used to support an external 25 MHz 1.2 V swing clock input through this pin.
J2.82	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J2.83	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J2.84	ETH_TRX3_P	---	---	---	IA/OA	Variable (See Note 2)	Ethernet Media Dependent Interface[3]. Route as 100-ohm differential pair with ENET_TRX3_N. Requires external magnetics.
J2.85	ETH_TRX1_N	---	---	---	IA/OA	Variable (See Note 2)	Ethernet Media Dependent Interface[1]. Route as 100-ohm differential pair with ENET_TRX1_P. Requires external magnetics.
J2.86	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J2.87	DGND	---	---	---	---	GND	Ground. Connect to digital ground.

J2 Pin#	Signal Name	BGA Ball#	Processor Signal	Processor Alternate Functions	I/O	Voltage (V)	Description
J2.88	ETH_TRX2_N	---	---	---	IA/OA	Variable (See Note 2)	Ethernet Media Dependent Interface[2]. Route as 100-ohm differential pair with ENET_TRX2_P. Requires external magnetics.
J2.89	ETH_TRX1_P	---	---	---	IA/OA	Variable (See Note 2)	Ethernet Media Dependent Interface[1]. Route as 100-ohm differential pair with ENET_TRX1_N. Requires external magnetics.
J2.90	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J2.91	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J2.92	ETH_TRX2_P	---	---	---	IA/OA	Variable (See Note 2)	Ethernet Media Dependent Interface[2]. Route as 100-ohm differential pair with ENET_TRX2_N. Requires external magnetics.
J2.93	ETH_TRX0_N	---	---	---	IA/OA	Variable (See Note 2)	Ethernet Media Dependent Interface[0]. Route as 100-ohm differential pair with ENET_TRX0_P. Requires external magnetics.
J2.94	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J2.95	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J2.96	I2C2_SDA	AE8	I2C2_SDA	I2C2_SDA, ENET_QOS_1588_EVENT1_OUT, USDHC3_WP, ECSPI1_SS0, GPIO5_IO17	I/O, OD	1.8	I2C2 Data. This signal has a 4.7k ohm pull-up.
J2.97	ETH_TRX0_P	---	---	---	IA/OA	Variable (See Note 2)	Ethernet Media Dependent Interface[0]. Route as 100-ohm differential pair with ENET_TRX0_N. Requires external magnetics.
J2.98	I2C2_SCL	AH6	I2C2_SCL	I2C2_SCL, ENET_QOS_1588_EVENT1_IN, USDHC3_CD_B, ECSPI1_MISO, ENET_QOS_1588_EVENT1_AUX_IN, GPIO5_IO16	I/O, OD	1.8	I2C2 Clock. This signal has a 4.7k ohm pull-up.
J2.99	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J2.100	DGND	---	---	---	---	GND	Ground. Connect to digital ground.

Table 32: J2 Baseboard Connector Pin Mapping

TABLE NOTES:

1. **MIPI CSI-2 voltage levels follow the MIPI CSI-2 specification. Please see the MIPI CSI-2 Specification for more information.**
2. **Ethernet voltage levels follow the Ethernet specification and depend on the Ethernet operating speed. Please see the IEEE 802.3 documentation for more information.**

13.3 J3 Baseboard Connector

J3 Pin#	Signal Name	BGA Ball#	Processor Signal	Processor Alternate Functions	I/O	Voltage (V)	Description
J3.1	VBUS2_DET_3V3	D12	USB2_VBUS	---	O, PWR	5	Universal Serial Bus 2 VBUS detect signal. This signal has a series 30k resistor to the processor on the SOM.
J3.2	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.3	GPIO2_IO10	W25	SD1_RESET_B	SD1_RESET_B, ENET1_TX_CLK, I2C3_SCL, UART3_RTS_B, GPIO2_IO10	O	1.8	Form factor usage: USB 2 ID Plus SOM: May be used as a GPIO.
J3.4	PCIE_CLKP	D16	PCIE_CLK_P	---	I	Variable (See Note 1)	PCIe Clock P. Route as 85-ohm differential pair with PCIE_CLKN.
J3.5	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.6	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.7	USB2_DN	E14	USB2_D_N	---	I/O	Variable (See Note 2)	Universal Serial Bus 2 Data N. Route as 90-ohm differential pair with USB2_DP.
J3.8	PCIE_CLKN	E16	PCIE_CLK_N	---	I	Variable (See Note 1)	PCIe Clock N. Route as 85-ohm differential pair with PCIE_CLKP.
J3.9	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.10	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.11	USB2_DP	D14	USB2_D_P	---	I/O	Variable (See Note 2)	Universal Serial Bus 2 Data P. Route as 90-ohm differential pair with USB2_DN.
J3.12	PCIE_TXN	B15	PCIE_TXN_N	---	I	Variable (See Note 1)	PCIe Transmit N. Route as 85-ohm differential pair with PCIE_TXP.
J3.13	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.14	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.15	USB1_DN	E10	USB1_DN	---	I/O	Variable (See Note 2)	Universal Serial Bus 1 Data N. Route as 90-ohm differential pair with USB2_DP.
J3.16	PCIE_TXP	A15	PCIE_TXN_P	---	I	Variable (See Note 1)	PCIe Transmit P. Route as 85-ohm differential pair with PCIE_TXN.
J3.17	DGND	---	---	---	---	GND	Ground. Connect to digital ground.

J3 Pin#	Signal Name	BGA Ball#	Processor Signal	Processor Alternate Functions	I/O	Voltage (V)	Description
J3.18	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.19	USB1_DP	D10	USB1_DP	---	I/O	Variable (See Note 2)	Universal Serial Bus 1 Data P. Route as 90-ohm differential pair with USB1_DN.
J3.20	PCIE_RXN	B14	PCIE_RXN_N	---	O	Variable (See Note 1)	PCIe Receive N. Route as 85-ohm differential pair with PCIE_RXP.
J3.21	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.22	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.23	USB1_VDET_3V3	A11	USB1_VBUS	---	O, PWR	5	Universal Serial Bus 1 VBUS detect signal. This signal has a series 30k resistor to the processor.
J3.24	PCIE_RXP	A14	PCIE_RXN_P	---	O	Variable (See Note 1)	PCIe Receive P. Route as 85-ohm differential pair with PCIE_RXN.
J3.25	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.26	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.27	MIPI_CSI1_DP3	D26	MIPI_CSI1_D3_P	---	O	See Note 3	MIPI CSI-2 Data 3 P. Route as 100-ohm differential pair with CSI1_DN3.
J3.28	MIPI_CSI1_DP2	D24	MIPI_CSI1_D2_P	---	O	See Note 3	MIPI CSI-2 Data 2 P. Route as 100-ohm differential pair with CSI1_DN2.
J3.29	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.30	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.31	MIPI_CSI1_DN3	E26	MIPI_CSI1_D3_N	---	O	See Note 3	MIPI CSI-2 Data 3 N. Route as 100-ohm differential pair with CSI1_DP3.
J3.32	MIPI_CSI1_DN2	E24	MIPI_CSI1_D2_N	---	O	See Note 3	MIPI CSI-2 Data 2 N. Route as 100-ohm differential pair with CSI1_DP2.
J3.33	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.34	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.35	MIPI_CSI1_CKP	D22	MIPI_CSI1_CLK_P	---	O	See Note 3	MIPI CSI-2 Clock P. Route as 100-ohm differential pair with CSI1_CKN.
J3.36	MIPI_CSI1_DP0	D18	MIPI_CSI1_D0_P	---	O	See Note 3	MIPI CSI-2 Data 0 P. Route as 100-ohm differential pair with CSI1_DN0.
J3.37	DGND	---	---	---	---	GND	Ground. Connect to digital ground.

J3 Pin#	Signal Name	BGA Ball#	Processor Signal	Processor Alternate Functions	I/O	Voltage (V)	Description
J3.38	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.39	MIPI_CSI1_CKN	E22	MIPI_CSI1_CLK_N	---	O	See Note 3	MIPI CSI-2 Clock N. Route as 100-ohm differential pair with CSI1_CKP.
J3.40	MIPI_CSI1_DN0	E18	MIPI_CSI1_D0_N	---	O	See Note 3	MIPI CSI-2 Data 0 N. Route as 100-ohm differential pair with CSI1_DP0.
J3.41	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.42	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.43	MIPI_CSI1_DP1	D20	MIPI_CSI1_D1_P	---	O	See Note 3	MIPI CSI-2 Data 1 P. Route as 100-ohm differential pair with CSI1_DN0.
J3.44	DSI_DP3	A20	MIPI_DSI1_D3_P	---	I	See Note 4	MIPI DSI Data 3 P. Route as 100-ohm differential pair with DSI_DN3.
J3.45	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.46	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.47	MIPI_CSI1_DN1	E20	MIPI_CSI1_D1_N	---	O	See Note 3	MIPI CSI-2 Data 1 N. Route as 100-ohm differential pair with CSI1_DP0.
J3.48	DSI_DN3	B20	MIPI_DSI1_D3_N	---	I	See Note 4	MIPI DSI Data 3 N. Route as 100-ohm differential pair with DSI_DP3.
J3.49	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.50	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.51	DSI_DP2	A19	MIPI_DSI1_D2_P	---	I	See Note 4	MIPI DSI Data 2 P. Route as 100-ohm differential pair with DSI_DN2.
J3.52	DSI_CKP	A18	MIPI_DSI1_CLK_P	---	I	See Note 4	MIPI DSI Clock P. Route as 100-ohm differential pair with DSI_CKN.
J3.53	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.54	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.55	DSI_DN2	B19	MIPI_DSI1_D2_N	---	I	See Note 4	MIPI DSI Data 2 N. Route as 100-ohm differential pair with DSI_DP2.
J3.56	DSI_CKN	B18	MIPI_DSI1_CLK_N	---	I	See Note 4	MIPI DSI Clock N. Route as 100-ohm differential pair with DSI_CKP.
J3.57	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.58	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.59	DSI_DP0	A16	MIPI_DSI1_D0_P	---	I	See Note 4	MIPI DSI Data 0 P. Route as 100-ohm differential pair with DSI_DN0.

J3 Pin#	Signal Name	BGA Ball#	Processor Signal	Processor Alternate Functions	I/O	Voltage (V)	Description
J3.60	DSI_DP1	A17	MIPI_DSI1_D1_P	---	I	See Note 4	MIPI DSI Data 1 P. Route as 100-ohm differential pair with DSI_DN1.
J3.61	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.62	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.63	DSI_DN0	B16	MIPI_DSI1_D0_P	---	I	See Note 4	MIPI DSI Data 0 N. Route as 100-ohm differential pair with DSI_DP0.
J3.64	DSI_DN1	B17	MIPI_DSI1_D1_P	---	I	See Note 4	MIPI DSI Data 1 N. Route as 100-ohm differential pair with DSI_DP1.
J3.65	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.66	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.67	ECSPI2_MISO	AH20	ECSPI2_MISO	ECSPI2_MISO, UART4_DCE_CTS, UART4_DTE_RTS, I2C4_SCL, SAI7_MCLK, CCM_CLK_01, GPIO5_IO12	O	1.8	Enhanced Configurable SPI 2 MISO
J3.68	JTAG_TMS	G14	JTAG_TMS	CJTAG_WRAPPER_TMS	O	1.8	JTAG TMS
J3.69	ECSPI2_MOSI	AJ21	ECSPI2_MOSI	ECSPI2_MOSI, UART4_DCE_TX, UART4_DTE_RX, I2C3_SDA, SAI7_TX_DATA00, GPIO5_IO11	I	1.8	Enhanced Configurable SPI 2 MOSI
J3.70	JTAG_TDI	G16	JTAG_TDI	CJTAG_WRAPPER_TDI	O	1.8	JTAG TDI
J3.71	UART3_CTS	AD20	ECSPI1_MISO	ECSPI1_MISO, UART3_DCE_CTS, UART3_DTE_RTS, I2C_SDL, SAI7_RX_DATA0, GPIO5_IO08	O	1.8	UART 3 Clear-To-Send
J3.72	JTAG_MOD	G20	JTAG_MOD	CJTAG_WRAPPER_MODE	O	1.8	Debug mode: JTAG_MOD == 0 DAP is the only TAP controller in the daisy chain. Test mode: JTAG_MOD == 1 SJC is the only TAP controller in the daisy chain. This signal has a 10k ohm pull-down.
J3.73	UART3_TXD	AC20	ECSPI1_MOSI	ECSPI1_MOSI, UART3_TX, UART3_DTE_RX, I2C1_SDA, SAI7_RX_BCLK, GPIO5_IO07	I	1.8	UART 3 Transmit
J3.74	USB1_TXN	B10	USB1_TXN	---	I	Variable (See Note 2)	USB1_TX N. Route as 90-ohm differential pair with USB1_TX P.
J3.75	ECSPI2_SS0	AJ22	ECSPI2_SS0	ECSPI2_SS0, UART4_DCE_RTS, UART4_DTE_CTS, I2C4_SDA, CCM_CLK02, GPIO5_IO13	I	1.8	Enhanced Configurable SPI 2 SS0
J3.76	USB1_TXP	A10	USB1_TXP	---	I	Variable (See Note 2)	USB1_TX P. Route as 90-ohm differential pair with USB1_TX N.
J3.77	UART3_RTS	AE20	ECSPI1_SS0	ECSPI1_SS0, UART3_DCE_RTS, UART3_DTE_CTS, I2C2_SDA, AUDIOMIX_SAI7_TX_SYNC, GPIO5_IO09	I	1.8	UART 3 Ready to Send

J3 Pin#	Signal Name	BGA Ball#	Processor Signal	Processor Alternate Functions	I/O	Voltage (V)	Description
J3.78	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.79	UART3_RXD	AF20	ECSPI1_SCLK	ECSPI1_SCLK, UART3_DCE_RX, UART3_DTE_TX, I2C1_SCL, SAI7_RX_SYNC, GPIO5_IO06	O	1.8	UART 3 Receive
J3.80	JTAG_TCK	G18	JTAG_TCK	CJTAG_WRAPPER_TCK	O	1.8	JTAG TCK.
J3.81	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.82	JTAG_TDO	F14	JTAG_TDO	CJTAG_WRAPPER_TDO	I	1.8	JTAG TDO
J3.83	ECSPI2_SCLK	AH21	ECSPI2_SCLK	ECSPI2_SCLK, UART4_RX, UART4_DTE_TX, I2C3_SCL, SAI7_TX_BCLK, GPIO5_IO10	I	1.8	Enhanced Configurable SPI 2 SCLK
J3.84	BOOT_MODE3	G12	BOOT_MODE3	---	O	1.8	BOOT_MODE3. See Section 5.1 for more information.
J3.85	BOOT_MODE2	G8	BOOT_MODE2	---	O	1.8	BOOT_MODE2. See Section 5.1 for more information.
J3.86	UART4_TXD	AH5	UART4_TXD	UART4_DCE_TX, UART4_DTE_RX, UART2_DCE_RTS, UART2_DTE_CTS, GPT1_CAPTURE1, I2C6_SDA, GPIO5_IO29	I	1.8	Serial UART 4 Transmit
J3.87	UART2_RXD	AF6	UART2_RXD	UART2_DCE_RX, UART2_DTE_TX , ECSPI3_MISO, GPT1_COMPARE3, GPIO5_IO24	O	1.8	Serial UART 2 Receive
J3.88	UART4_RXD	AJ5	UART4_RXD	UART4_DCE_RX, UART4_DTE_TX, UART2_DCE_CTS , UART2_DTE_RTS, PCIE_CLKREQ_B, GPT1_COMPARE1, I2C6_SCL, GPIO5_IO28	O	1.8	Serial UART 4 Receive
J3.89	UART2_TXD	AH4	UART2_TXD	UART2_DCE_TX, UART2_DTE_RX, ECSPI3_SS0, GPT1_COMPARE2, GPIO5_IO25	I	1.8	Serial UART 2 Transmit
J3.90	GPIO1_IO00	A7	GPIO1_IO00	GPIO1_IO00, CCM_ENET_PHY_REF_CLK_ROOT, ISP_FL_TRIG_0, ANAMIX_REF_CLK_32K, CCM_EXT_CLK1	I/O	1.8	32KHz Ref Clock or may be used as GPIO.
J3.91	USB2_TXP	A13	USB2_TX_P	---	I	Variable (See Note 2)	USB2 TX2 P. Route as 90-ohm differential pair with USB2_TX_N.
J3.92	USB1_RXN	B9	USB1_RX_N	---	O	Variable (See Note 2)	USB1 RX N. Route as 90-ohm differential pair with USB1_RX_P.
J3.93	USB2_TXN	B13	USB2_TX_N	---	I	Variable (See Note 2)	USB2 TX N. Route as 90-ohm differential pair with USB2_TX_P.
J3.94	USB1_RXP	A9	USB1_RX_P	---	O	Variable (See Note 2)	USB1 RX P. Route as 90-ohm differential pair with USB1_RX_N.

J3 Pin#	Signal Name	BGA Ball#	Processor Signal	Processor Alternate Functions	I/O	Voltage (V)	Description
J3.95	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.96	SOM_DETECT	---	---	---	---	GND	SOM_DETECT is pulled high (3.3V) when i.MX mini/nano SOM is used SOM_DETECT is grounded when i.MX Plus SOM is used
J3.97	VBACKUP	---	---	---	PWR	3.3 or coin cell	Battery Backup. Provide a voltage of +0.9V to +5.5V on this rail. If RTC functionality is required, this supply must be always kept on. Note: X1 coin cell must be disconnected before applying any external voltage to VBACKUP.
J3.98	USB2_RXN	B12	USB2_RX_N	---	O	Variable (See Note 2)	USB2 RX N. Route as 90-ohm differential pair with USB2_RX_P.
J3.99	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J3.100	USB2_RXP	A12	USB2_RX_P		O	Variable (See Note 2)	USB2 RX P. Route as 90-ohm differential pair with USB2_RX_N.

Table 33: J3 Baseboard Connector Pin Mapping

TABLE NOTES:

1. **PCIe voltage levels follow the PCIe specification and depend on the operating speed. Please see PCI-SIG for more information.**
2. **USB voltage levels follow the USB specification and depend on the USB operating speed. Please see the USB 2.0 Specification for more information.**
3. **MIPI CSI-2 voltage levels follow the MIPI CSI-2 specification. Please see the MIPI CSI-2 Specification for more information.**
4. **MIPI DSI voltage levels follow the MIPI DSI specification. Please see the MIPI DSI Specification for more information.**

13.4 J4 Baseboard Connector

J3 Pin#	Signal Name	BGA Ball#	Processor Signal	Processor Alternate Functions (See Note 5)	I/O	Voltage (V)	Description
J4.1	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J4.2	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J4.3	LVDS1_CLK_N	B28	LVDS1_CLK_N	---	I	See Note 1	LVDS1 CLK N. Route as 100-ohm differential pair with LVDS1_CLK_P.
J4.4	LVDS1_D0_N	B26	LVDS1_D0_N	---	I	See Note 1	LVDS1 DATA0 N. Route as 100-ohm differential pair with LVDS1_D0_P.
J4.5	LVDS1_CLK_P	A28	LVDS1_CLK_P	---	I	See Note 1	LVDS1 CLK P. Route as 100-ohm differential pair with LVDS1_CLK_N.
J4.6	LVDS1_D0_P	A26	LVDS1_D0_P	---	I	See Note 1	LVDS1 DATA0 P. Route as 100-ohm differential pair with LVDS1_D0_N.
J4.7	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J4.8	LVDS1_D1_N	B27	LVDS1_D1_N	---	I	See Note 1	LVDS1 DATA1 N. Route as 100-ohm differential pair with LVDS1_D1_P.
J4.9	WLAN_COEX_SOUT				I	1.8	WiFi serial data to external LTE device
J4.10	LVDS1_D1_P	A27	LVDS1_D1_P	---	I	See Note 1	LVDS1 DATA1 P. Route as 100-ohm differential pair with LVDS1_D1_N.
J4.11	WLAN_COEX_SIN				O	1.8	WiFi serial data from external LTE device
J4.12	LVDS1_D2_N	C28	LVDS1_D2_N	---	I	See Note 1	LVDS1 DATA2 N. Route as 100-ohm differential pair with LVDS1_D2_P.
J4.13	BT_LED				I	1.8	Bluetooth Activity
J4.14	LVDS1_D2_P	B29	LVDS1_D2_P	---	I	See Note 1	LVDS1 DATA2 P. Route as 100-ohm differential pair with LVDS1_D2_N.
J4.15	WLAN_LED				I	1.8	WiFi Activity
J4.16	LVDS1_D3_N	D28	LVDS1_D3_N	---	I	See Note 1	LVDS1 DATA3 N. Route as 100-ohm differential pair with LVDS1_D3_P.
J4.17	---	---	---	---	---	---	Reserved for future use. Do not connect.
J4.18	LVDS1_D3_P	C29	LVDS1_D3_P	---	I	See Note 1	LVDS1 DATA3 P. Route as 100-ohm differential pair with LVDS1_D3_N.
J4.19	DGND	---	---	---	---	GND	Ground. Connect to digital ground.
J4.20	DGND	---	---	---	---	GND	Ground. Connect to digital ground.

Table 34: J4 Baseboard Connector Pin Mapping

TABLE NOTES:

1. **LVDS voltage levels follow the LVDS specification. Please see TIA/EIA STANDARD 644-A standard for more information.**

Appendix A: Additional Documentation

Software Documentation[9]

i.MX 8M Plus YOCTO Linux BSP User Guide

Hardware Documentation[9]

Beacon's i.MX 8M Plus Development Kit Quick Start Guide
Beacon's i.MX 8M Plus SOM Product Brief
Beacon's i.MX 8M Plus SOM Hardware Specification

[9] May require a Beacon EmbeddedWorks login account and product registration to download Beacon EmbeddedWorks documents.