OMAP35x SOM-LV Hardware Specification

Hardware Documentation

Logic PD // Products
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Revision History

REV	REVISION DESCRIPTION	SCHEMATIC PN & REV	APPROVAL	DATE
1	Internal Release	1007969 Rev 8	NJK	04/28/08
A	-Throughout: Updated Triton2 name to TPS65950; -Section 3: Added note about regulators; -Section 4.2.1: Updated memory options; -Sections 4.4, 4.5, & 4.9: Updated component part numbers; -Section 7.1: Changed max voltage for touch screen signals to 3.1 V -Section 5.2: Added note about SIM interface for respective signal descriptions; -Section 6: Clarified measurement tolerances -Section 6: Updated diagram so that it only shows footprint for SOM-LV Type III	1007969 Rev 8	NJK	06/05/08
B	-Added standard document cover page; updated header and footer layout; -Figure 2.2: Removed USB HS OTG signal coming from USB PHY x1; -Table 3.1: Added voltage ratings for 5V supply; the current values were given in Amps when they should be in mA, this has been corrected; Removed note about regulators; -Section 4.9 & throughout: USB host can only operate in high-speed; -Section 5.4: Added MSTR_nRST signal to JTAG interface explanation; -Section 5.6.1: Added note about USB1_VBUS powering the SOM; -Section 6: For nCS2 chip select, removed the word "boot" from the device field. -Section 7.1: Pin J1.153 was "RFU", updated to "LCD_DON"; -Section 7.2: Pin J2.44 changed parenthetical net name from "VIO_1V8" to "uP_LA12"; pins J2.156, 158, 160, 162, 164, & 166 updated descriptions to explain GPIO is not available when Bluetooth is populated; pinJ2.168 updated description by removing the words "boot" and "bootselect"; added note about uP_nCS0 tied to uP_nCS2; pins J2.237-240 updated signal names used for test, used to be listed as "RFU"; for "CSI1_xxx" signals, updated the description to indicate that the Camera Serial Interface is not natively supported on the OMAP35x processor; -Section 0: Added section for Wireless Antenna Connectors; Updated Mechanical Drawings	1009917 Rev A	NJK & JCA	09/08/08
C	-Sections 4.4 & 4.5: Specified wireless antenna connector locations on PCB; -Section 6: Added note about chip select memory locations -Section 7.1: Corrected J1 connector processor data bits to be I/O signals	1009917 Rev A	NJK	10/29/08
D	- Figure 2.2: Updated Block Diagram; - Added Section 4.2.3.1: Example CompactFlash Timing; - Section 4.9: Updated for new USB host controller, which adds USB high-speed ports that support more than high-speed mode; - Section 4.13: Added design note about the GPMC bus; - Section 6: Added nCS6 to table - Section 7.1: Updated voltages on pins J1.37, 39 for USB changes; Updated descriptions for pins J1.131 & 133; pin J1.135 changed from uP_DREQ1 to RFU; pins J1.141, 143, 145, & 147 were updated to include nCS4/nCS5; pins J1.174, 176, & 178 updated description; pins J1.233, 235, 237, 239, & 240 changed from RFU to used for testing; - Section 7.2: Pins J2.58, 60, 62, 64, 70, 74, 76, & 78 changed from RFU to being used by new USB features; pin J2.87 added Note 1 at the conclusion of table; pin J2.175 added required capacitance note;	1010913 Rev B	NJK	01/20/09
E	- Throughout: Updated URLs where necessary; - Section 2.2: Used updated look for block diagram; - Section 3: Added Extended Temperature range; corrected dimensions; - Section 5.2.1: Added Important Note that MSTR_nRST does not reset PMIC; - Section 5.5: Added Important Note about ETM interface speeds; - Section 7.1: J1.23,37 & J2.58,70 noted external 10K pull-up resistor to 3.3V requirement for all nOC pins; - Added Section 2.3.3; - Appendix A: Updated drawing	1010913 Rev C	JCA	09/02/09
F	- Section 7: Added Important Note concerning power rails for GPIOs; - Section 7.2: J2.181, 183, 185, 187 changed to GPI only; J2.133, 135 added can be used as GPI	1010913 Rev C	BSB & NJK	10/26/09

REV	REVISION DESCRIPTION	SCHEMATIC PN & REV	APPROVAL	DATE
G	- Section 3: Updated DC 5 V Voltage Min & Typical numbers; Added notes 7-9 to explain how the power numbers were obtained; - Section 4.8.5.1: Added list of reserved I2C addresses; - Section 7: Updated important note to remove reference to LogicLoader; - Section 7.1: J1.113, 115 added notes about signals used with SD cards; - Section 7.2: J2.133, 135, 181, 183, 185, 187 changed voltage to reference VAUX4 and updated Notes; J2.233 added note that this signal is shared with Bluetooth;	1010913 Rev C	RH & NJK	04/21/10
H	- Section 3: Added 802.11 numbers; Added numbers for Active Current running WinCE BSP; Updated typical numbers for active currents; Updated extended temperature range; - Section 4.3: Added note about baseboard Ethernet socket contains integrated magnetics; - Section 4.4: Added information for the Murata module; - Section 4.9: Added information about USB transceiver; - Sections 4.11 & 4.13: Added design note; - Section 6: Removed nCS6 from chip select table; - Section 7: Added notes for specific PoP signals; Organized notes and moved several multi-signal notes to end of tables instead of in descriptions; - Section 7.1: Updated descriptions for J1.23, 25; Corrected voltage level and updated descriptions for J1.37, 39; Changed pins J1.233, 235, 239, & 240 to use used as Wireless signals instead of SPI_*; - Section 7.2: Corrected voltage level and updated descriptions for J2.58, 60, 70, 78; Changed pins J2.81, 83 to RFU; Updated description for pin J2.175	1014465 Rev A	NJK	11/03/10
I	-Sections 3, 7.1, & 7.2: Changed Max DC Main Battery Input Voltage to 4.3V as a result of the wireless module limits; -Section 4.9: Revised incorrect USB reference; -Section 5.6.1.3: Added Important Note about 3.3V rail required for Ethernet and USB; -Section 7.1 & 7.2 Added BGA Ball # and Processor Signal columns to tables -Section 2.3.2: Added antenna part number included in dev kit; Added separate table for connector information	1014465 Rev A	NJK	09/12/11
J	-Appendix A: Added updated mechanical drawing that includes connector pin orientations	1014465 Rev A	SO	06/19/12
K	-Throughout: Updated template; updated links for new support site; reorganized several sections; -Section 4.9: Added note that proper USB adapter cable is necessary for USB 2.0 OTG to function as host; added link to Digi-Key adapter cable that supports host function; -Section 7.2: Changed I/O column to output only and added *open drain* to descriptions for J2:93, J2:95, J2:97, J2:99, J2:101, J2:103, J2:105, J2:107; changed I/O column to input only for J2:109, J2:113, J2:115, J2:117, J2:119, J2:121, J2:123, J2:125, J2: 151, J2:153, J2:155, J2:157, J2:171, J2:181, J2:183, and J2:187	1014465 Rev B	SO, BSB	11/14/13
L	-Section 4.2.2: Documented change from 8MB Strataflash NOR to 16MB NOR Embedded Memory.	1028918 Rev A-0	JMC	08/23/17

Please check the Logic PD support site[1] for the latest revision of this specification and additional documentation.

[1] http://support.logicpd.com/Home.aspx

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1 Introduction

1.1 Product Overview

The OMAP35x System on Module (SOM) is a compact, product-ready hardware and software solution that fast forwards embedded designs.

Based on the Texas Instruments (TI) OMAP35x processor and designed in the SOM-LV Type III form factor, the OMAP35x module offers essential features for handheld and embedded networking applications.

The SOM-LV is an off-the-shelf solution that reduces development risks associated with the complex design and manufacturing details of the OMAP 3 processor. The standard SOM-LV form factor allows developers to reuse existing baseboard designs when upgrading to new OMAP processors, which extends roadmap possibilities for their end-product. By starting with the corresponding Zoom™ OMAP35x Development Kit, engineers can write application software on the same hardware that will be used in the final product.

The OMAP35x SOM-LV is ideal for applications in the medical, point-of-sale, industrial, gaming, and security markets. From patient monitoring and medical imaging, to card payment terminals and bar code readers, to CCTV cameras and intruder alarms, the OMAP35x SOM-LV allows for powerful versatility and long-life products.

NOTE: Within this document, OMAP35x is used to denote any TI OMAP processor from the OMAP35x family (i.e., OMAP3530, OMAP3525, OMAP3515, and OMAP3503).

1.2 Abbreviations, Acronyms, and Definitions

ADC	Analog to Digital Converter
BSP	Board Support Package
BTB	Board-to-Board
DDR	Double Data Rate (RAM)
DMA	Direct Memory Access
ESD	Electrostatic Discharge
FIFO	First In First Out
GPIO	General Purpose Input Output
GPMC	General Purpose Memory Controller
GPO	General Purpose Output
I2C	Inter-Integrated Circuit
I2S	Inter-Integrated Circuit Sound
IC	Integrated Circuit
I/O	Input/Output
IRQ	Interrupt Request
LCD	Liquid Crystal Display
LDO	Low Dropout (Regulator)
McBSP	Multi-channel Buffered Serial Port
OTG	On-the-Go (USB)
PCB	Printed Circuit Board
PCMCIA	Personal Computer Memory Card International Association (PC Cards)
PHY	Physical Layer
PLL	Phase Lock Loop
POP	Package On Package

PWM	Pulse Width Modulation
RTC	Real Time Clock
SDIO	Secure Digital Input Output
SDRAM	Synchronous Dynamic Random Access Memory
SOM	System on Module
SSP	Synchronous Serial Port
SPI	Standard Programming Interface
STN	Super-Twisted Nematic (LCD)
TFT	Thin Film Transistor (LCD)
TI	Texas Instruments
TSC	Touch Screen Controller
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receive Transmit

1.3 Scope of Document

This hardware specification is unique to the design and use of the OMAP35x SOM-LV as designed by Logic PD and does not intend to include information outside of that scope. Detailed information about the TI OMAP35x processors or any other device component on the SOM can be found in their respective manuals and specification documents.

1.4 Additional Documentation and Resources

The following documents and documentation resources have been referenced throughout this hardware specification:

- TI's *OMAP35x Technical Reference Manual (TRM)*[2]
- TI's *OMAP3530/25 Applications Processor Datasheet*[2]
- TI's *TPS65950 OMAP Power Management and System Companion Device TRM*[3]
- TI's *TPS65950 Data Manual*[3]
- TI'S *TSC2004 Datasheet*[4]
- *USB 2.0 Specification*[5] available from USB.org
- Logic PD's *LogicLoader v2.4 User Manual*[6]
- Logic PD's *OMAP35x SOM-LV LogicLoader User Manual Addendum*[7]
- Logic PD's *AN 388 OMAP35x SOM-LV Power Management*[8]
- Logic PD's Hardware Design Files (BOM, Schematic, and Layout) for all boards included in the development kit (baseboard, SOM, LCD), as well as all standard configuration SOMs. Sign into your account on Logic PD's support site[9] to access these files.

[2] http://www.ti.com/product/omap3530
[3] http://www.ti.com/product/tps65950#technicaldocuments
[4] http://www.ti.com/product/tsc2004
[5] http://www.usb.org/developers/docs/
[6] http://support.logicpd.com/DesktopModules/Bring2mind/DMX/Download.aspx?portalid=0&EntryId=1455
[7] http://support.logicpd.com/DesktopModules/Bring2mind/DMX/Download.aspx?portalid=0&EntryId=1126
[8] http://support.logicpd.com/DesktopModules/Bring2mind/DMX/Download.aspx?portalid=0&EntryId=1108
[9] http://support.logicpd.com/Home.aspx

2 Functional Specification

2.1 OMAP35x Processor Highlights

The OMAP35x SOM-LV uses TI's high-performance OMAP35x processor. This device features the Superscalar ARM® Cortex™-A8 RISC core and provides many integrated on-chip peripherals, including:

- Superscalar ARM® Cortex™-A8 RISC core
  - Vectored floating point unit
  - 16 Kbytes instruction L1 cache
  - 16 Kbytes data L1 cache
  - 256 Kbyte L2 cache
  - 64 Kbyte RAM
  - 32 Kbyte ROM
- Integrated LCD Controller
  - Up to 1024 x 768 x 24 bit color
- Three UARTs
- I2S codec interface
- One high-speed USB 2.0 On-the-Go (OTG) interface and one high-speed USB 2.0 host interface
- Many general purpose I/O (GPIO) signals
- Programmable timers
- Real time clock (RTC)
- Low power modes

See TI's *OMAP35x TRM* and *OMAP3530/25 Applications Processor Datasheet* for additional information.

IMPORTANT NOTE: Please visit TI's website[10] for errata on the OMAP35x processor.

[10] http://www.ti.com/product/omap3530

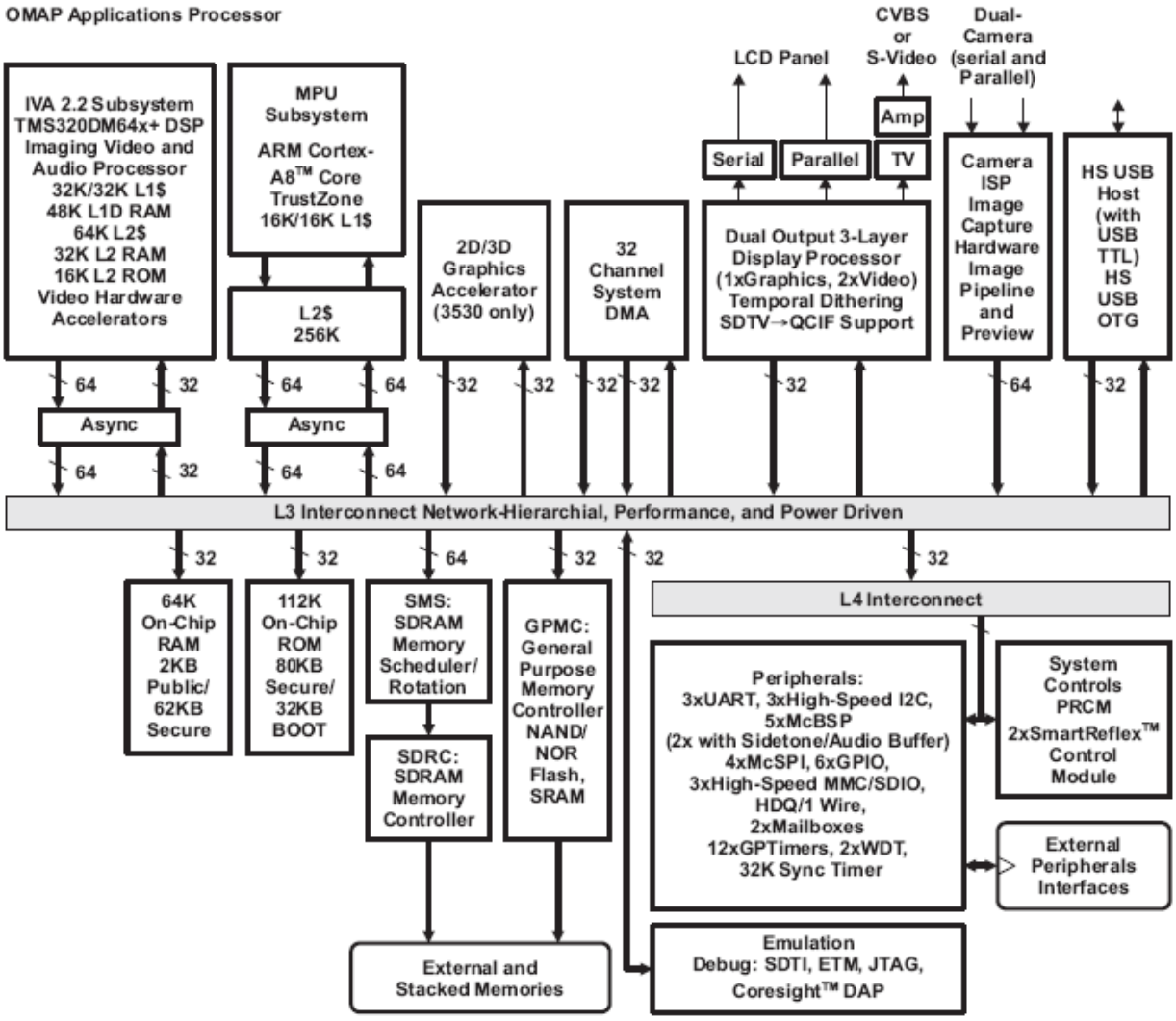


Figure 2.1: OMAP35x Processor Block Diagram

NOTE: The block diagram pictured above comes from TI's *OMAP3530/25 Applications Processor Datasheet.*

2.2 SOM-LV Interface

Logic PD's common SOM-LV interface allows for easy migration to new processors and technology. Logic PD is constantly researching and developing new technologies to improve performance, lower cost, and increase feature capabilities. By using the common SOM-LV footprint, it is possible to take advantage of Logic PD's work without having to re-spin the old design in certain cases dependent upon peripheral usage.

In fact, encapsulating a significant amount of your design onto the SOM-LV reduces any long-term risk of obsolescence. If a component on the SOM-LV design becomes obsolete, Logic PD will simply design for an alternative part that is as transparent to your product as possible. Furthermore, Logic PD tests all SOMs prior to delivery, decreasing time-to-market

and ensuring a simpler and less costly manufacturing process. Contact Logic PD[11] for more information.

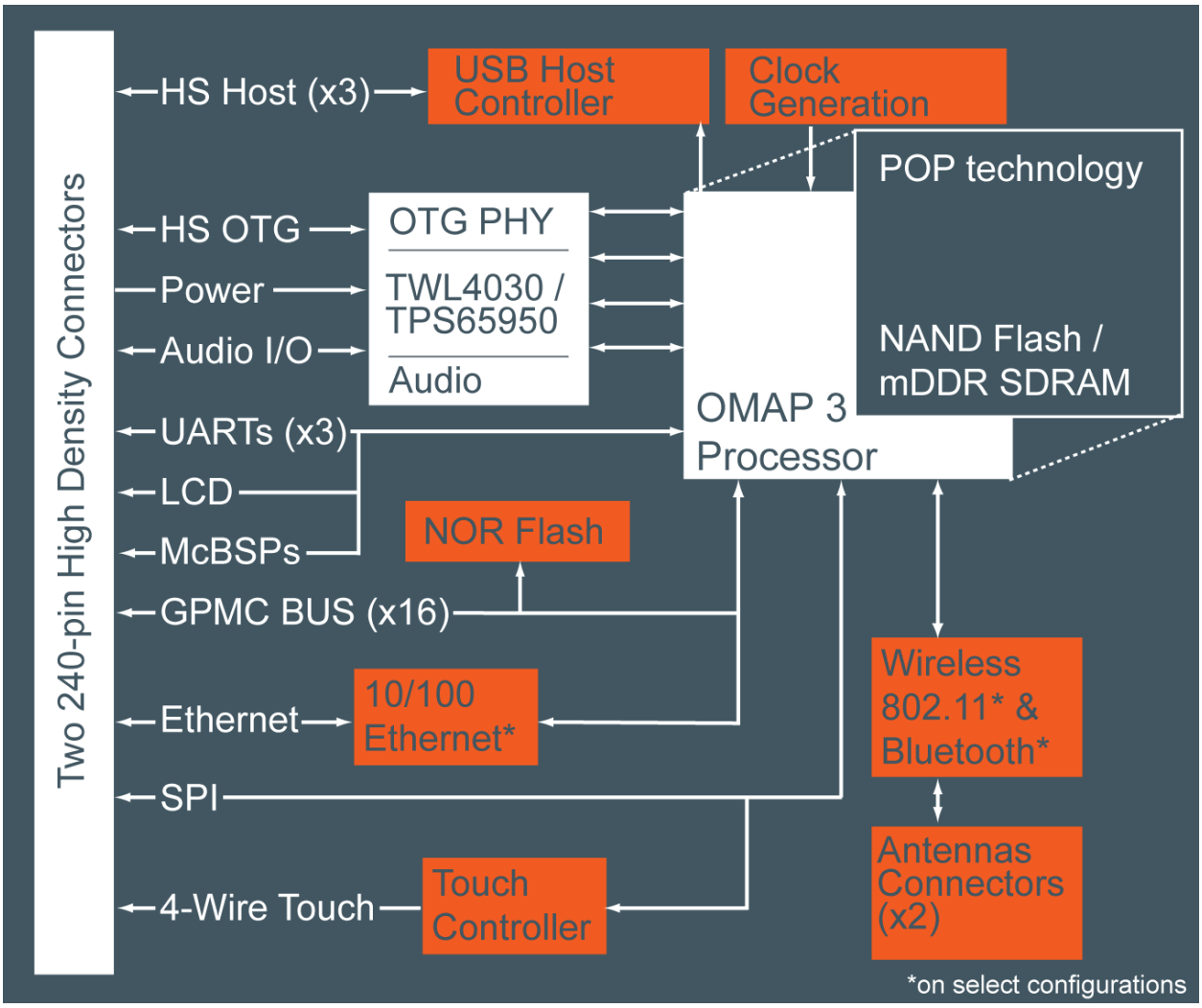


Figure 2.2: OMAP35x SOM-LV Block Diagram

[11] http://support.logicpd.com/TechnicalSupport/AskAQuestion.aspx

2.3 Mechanical Specification

2.3.1 Interface Connectors

The OMAP35x SOM-LV connects to a PCB baseboard through two 240-pin board-to-board (BTB) socket connectors.

Table 2.1: Baseboard Mating Connectors

Ref Designator	Manufacturer	OMAP35x SOM-LV Connector P/N	Mating Connector P/N
J1, J2	Samtec	BTH-120-01-L-D-A	BSH-120-01-L-D-A

2.3.2 Wireless Antenna Connectors

The OMAP35x SOM-LV mechanical drawings in Appendix A show the locations of the 802.11b/g/n Ethernet and Bluetooth antenna connectors on the top side of the PCB.

Table 2.2: Antenna PCB Connectors

Ref Designator	Manufacturer	P/N
J3, J4	Hirose	U.FL-R-SMT

The table below contains the manufacturer information for the cables and antenna that Logic PD provides in the OMAP35x Development Kit.

Table 2.3: Antennas Included in Development Kit

Ref Designator	Manufacturer	P/N
Antenna Cable	Sunridge Corporation	MCBG-RH-54-080-SMAJB281
Antenna	Pulse Engineering	W1030

2.3.3 Mounting Specifications

Attach spacers between the OMAP35x SOM-LV and the baseboard to provide additional support when securing the OMAP35x SOM-LV to the baseboard.

Table 2.4: Support Spacers to Secure OMAP35x SOM-LV to Baseboard

Manufacturer	PN	Description
Bivar	9908-5MM	Nylon screw (#4) spacers, 5 mm

Securing the OMAP35x SOM-LV to the baseboard requires screws of size 3 or smaller.

Only use flat washers with diameters of 3.8 mm or smaller when securing the OMAP35x SOM-LV to the baseboard. Any other washer type or size may result in cut traces or component and PCB damage leaving the OMAP35x SOM-LV inoperable.

IMPORTANT NOTE: Do not apply an excessive amount of torque when securing the OMAP35x SOM-LV to the baseboard. Using more torque than necessary may damage the OMAP35x SOM-LV.

2.3.4 OMAP35x SOM-LV Mechanical Drawings

Please see Appendix A for mechanical drawings of the OMAP35x SOM-LV and recommended baseboard footprint layout.

3 Electrical Specification

Table 3.1: Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
DC 3.3 V Supply Voltage	3.3V	0.0 to 3.6	V
DC 5 V Supply Voltage	5V	0.0 to 7.0	V
DC Main Battery Input Voltage	MAIN_BATTERY	0.0 to 4.5	V
RTC Backup Battery Voltage	BACKUP_BATT	0.0 to 3.3	V

NOTE: These stress ratings are only for transient conditions. Operation at or beyond absolute maximum rating conditions may affect reliability and cause permanent damage to the OMAP35x SOM-LV and its components.

Table 3.2: Recommended Operating Conditions

Parameter	Min	Typical	Max	Unit	Notes
DC Main Battery Input Voltage	**2.7*** (see note 11)	3.3	4.3	V	11
DC Main Battery Active Current	—	300	—	mA	4
DC Main Battery Active Current	—	234	—	mA	5
DC Main Battery Active Current	—	162	—	mA	6
DC Main Battery Suspend Current	—	102	—	mA	7
DC Main Battery Standby Current	—	—	—	mA	
DC 3.3 V Voltage	3.0	3.3	3.6	V	
DC 3.3 V Active Current	—	118	—	mA	4
DC 3.3 V Active Current	—	58	—	mA	5
DC 3.3 V Active Current	—	120	—	mA	6
DC 3.3 V Suspend Current	—	88	—	mA	7
DC 3.3 V Standby Current	—	—	—	mA	
DC 5 V Voltage	4.6	4.6	7.0	V	8,9,10
DC RTC Backup Battery Voltage	1.8	3.2	3.3	V	
802.11b Transmit Power	+16	+18	+20	dBm	12
802.11b Receive Sensitivity	—	-87	-76	dBm	12
802.11g Transmit Power	+11	+13	+15	dBm	12
802.11g Receive Sensitivity	—	-73	-68	dBm	12
802.11n Transmit Power	+10	+12	+14	dBm	12
802.11n Receive Sensitivity	—	-67	-64	dBm	12
Commercial Operating Temperature	0	25	70	°C	
Extended Operating Temperature	-20	—	70	°C	
Industrial Operating Temperature	-40	—	85	°C	
Storage Temperature	-40	25	85	°C	
Dimensions	—	31.2 x 76.45 x 7.4	—	mm	

Parameter	Min	Typical	Max	Unit	Notes
Weight	—	17	—	Grams	2
Connector Insertion/Removal	—	50	—	Cycles	
Input Signal High Voltage	0.65 x VREF	—	VREF	V	3
Input Signal Low Voltage	-0.3	—	0.35 x VREF	V	3
Output Signal High Voltage	VREF - 0.2	—	VREF	V	3
Output Signal Low Voltage	GND	—	0.2	V	

TABLE NOTES:

1. General note: CPU power rails are sequenced on the module.
2. May vary depending on OMAP35x SOM-LV configuration.
3. VREF represents the peripheral I/O supply reference for the specific CPU voltage rail.
4. Full Run [Active], while(1) loop in LogicLoader v2.4.13P1 on a fully-populated OMAP35x SOM-LV. No peripherals attached.
5. Full Run [Active], Linux BSP v2.6.32-bsp-2.1 on a fully-populated OMAP35x SOM-LV. No peripherals attached.
6. Full Run [Active], Windows CE BSP v2.0.1 on a fully-populated OMAP35x SOM-LV. No peripherals attached.
7. Suspend current is measured while running Windows CE BSP v2.0.1 after pushing the S2 button on the SDK2-APP-10 baseboard to enter suspend mode.
8. Please see Section 5.6.1.2 for detailed information about 5V usage on the OMAP35x SOM-LV.
9. The minimum voltage value of the charging device is:VBATMAX + 2 PMOS drop + 0.22 ohm resistor drop (where VBATMAX is the maximum voltage value of the battery; that is, 4.2V for Li-ion battery)
10. High input voltage levels may limit the charging capabilities of the OMAP35x SOM-LV. Please reference Logic PD's *OMAP35x SOM-LV Power Management Application Note* for more information.
11. 2.7V is the minimum threshold for the battery at which the device will power OFF. However, the minimum voltage at which the device will power ON is 3.2V ±100mV (if PWRON does not have a switch and is connected to MAIN_BATTERY) considering battery plug as the device switch on event. If PWRON has a switch then 3.2V is the minimum for the device to power ON.
12. Wireless numbers taken from the Murata LBEH19XMMC Module Datasheet (Rev. I). Logic PD is working to verify these numbers using the OMAP35x SOM-LV.

4 Peripheral Specification

4.1 Clocks

The OMAP35x processor requires an oscillator and crystal to enable proper internal timing. A 26.000 MHz oscillator is used to generate many of the processor's internal clocks via a series of Phase Lock Loops (PLLs) and signal dividers. To generate the core CPU clock, the 26.000 MHz signal is run through a Digital PLL controlled by the PRCM registers. Divisors are used to divide down the internal bus frequency to set the LCD, memory controller, camera interface, etc.

IMPORTANT NOTE: Please see TI's *OMAP35x TRM* for additional information about processor clocking.

The second required crystal runs at 32.768 kHz and is connected directly to the TPS65950. The 32.768 kHz clock is used for PMIC and CPU start up and as a reference clock for the real time clock (RTC) module.

The CPU's microcontroller core clock speed is initialized by software on the OMAP35x SOM-LV. The SDRAM bus speed is set at 166 MHz in LogicLoader. Other clock speeds, such as core speed and specific serial baud rates, can be supported and modified in software for specific user applications.

The OMAP SOM-LV provides an external bus clock, uP_BUS_CLK. This clock is driven by the GPMC_CLK pin.

Table 4.1: Processor Clock Specifications

OMAP35x Microcontroller Signal Name	OMAP35x SOM-LV Net Name	Default Software Value in LogicLoader
CORE	N/A	Up to 600 MHz
SDRC_CLK	SDRC_CLK	166 MHz
GPMC_CLK	uP_BUS_CLK	Not configured

4.2 Memory

4.2.1 Package-on-Package Memory (Mobile DDR and NAND)

The OMAP35x processor uses Package-on-Package (PoP) technology to stack BGA memory devices on top of the CPU BGA. The processor uses a 32-bit memory bus to interface to mobile DDR (mDDR) SDRAM and a 16-bit memory bus to interface to NAND. The PoP devices can be ordered with the following density options:

- 128 MB mDDR and 256 MB NAND
- 256 MB mDDR and 512 MB NAND

Logic PD's default memory configuration on the OMAP35x SOM-LV included in the OMAP35x Development Kit is specified as 128 MB mDDR and 256 MB NAND.

4.2.2 NOR Flash

The OMAP35x SOM-LV uses the 16-bit GPMC memory bus to interface to a single NOR flash memory chip. The onboard SOM-LV NOR flash memory can be configured as 0, 8, 16, 32, or 64 MB to meet the user's flash requirements and cost constraints. Logic PD's default flash configuration is 16 MB on the OMAP35x SOM-LV included in the standard OMAP35x Development Kit. Because flash is one of the most expensive components on the OMAP35x SOM-LV, it is important to contact Logic PD when determining the necessary flash size for final product configuration. NAND flash is a lower cost alternative that should be considered for final product configuration.

It is possible to expand the system's non-volatile storage capability by adding external flash ICs, SD memory, CompactFlash, or NAND flash. Please contact Logic PD for other possible peripheral designs.

4.2.3 PC Card Interface

The OMAP35x CPU does not directly support PCMCIA or CompactFlash slots. The OMAP35x SOM-LV uses internal logic to provide the necessary signals for the CompactFlash interface, creating support for a single external memory-mode only CompactFlash card. The OMAP35x Development Kit reference design includes a hot-swappable CompactFlash connector. Additional CompactFlash slots can be added using the GPMC bus. For more information on implementing additional slots, contact Logic PD.

4.2.3.1 Example CompactFlash Timing

On the OMAP35x SOM-LV, the CompactFlash interface (nCS3 of the GPMC bus) is set up with the following register settings:

```
0x6e00_00f0 0x0000_1210
0x6e00_00f4 0x0013_1000
0x6e00_00f8 0x001F_1F01
0x6e00_00fC 0x1003_0E03
0x6e00_0100 0x010F_1411
0x6e00_0104 0x8003_0600
0x6e00_0108 0x0000_0F58
```

These settings yield the following timing diagrams, which conform to the *CompactFlash Specification Revision 3.0*.

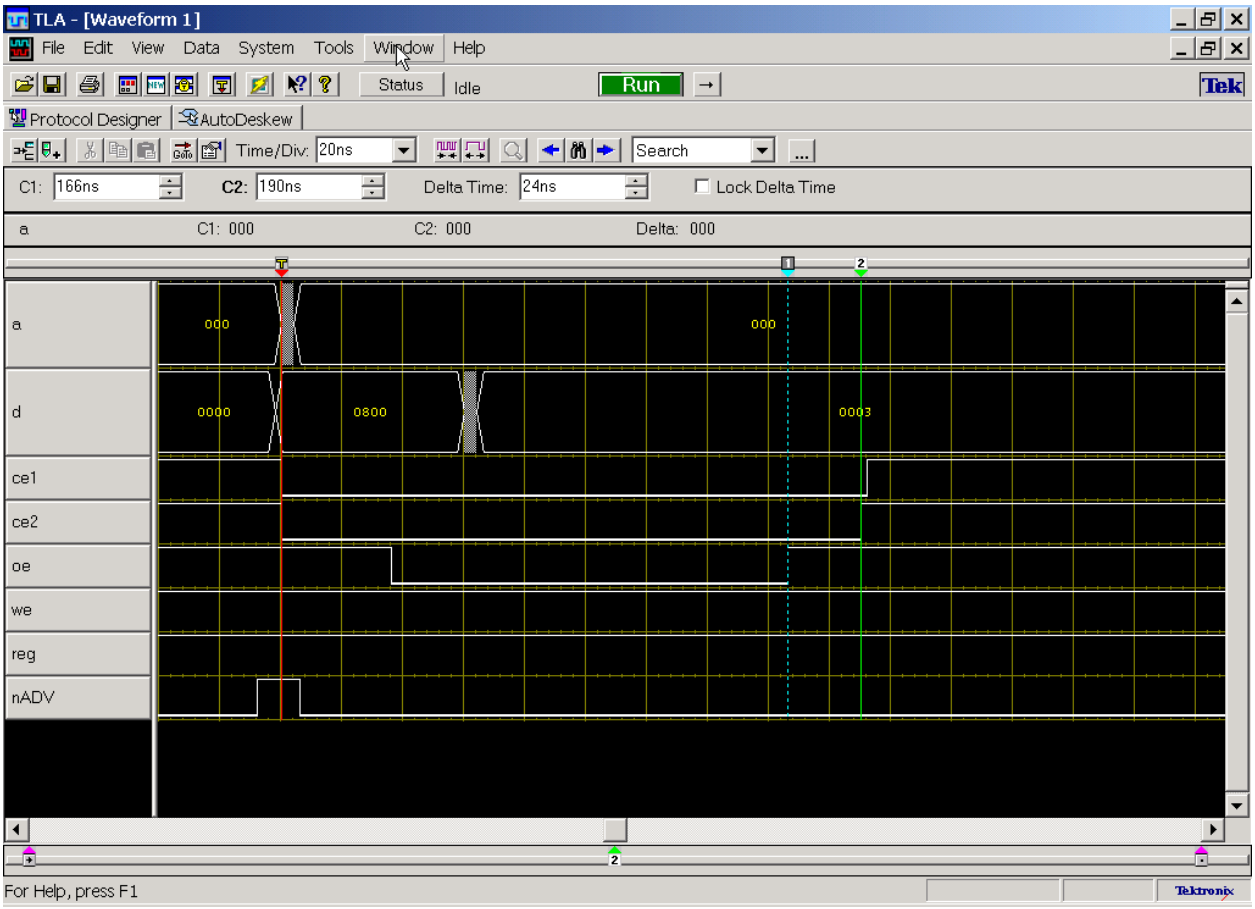


Figure 4.1: CompactFlash Read Timing

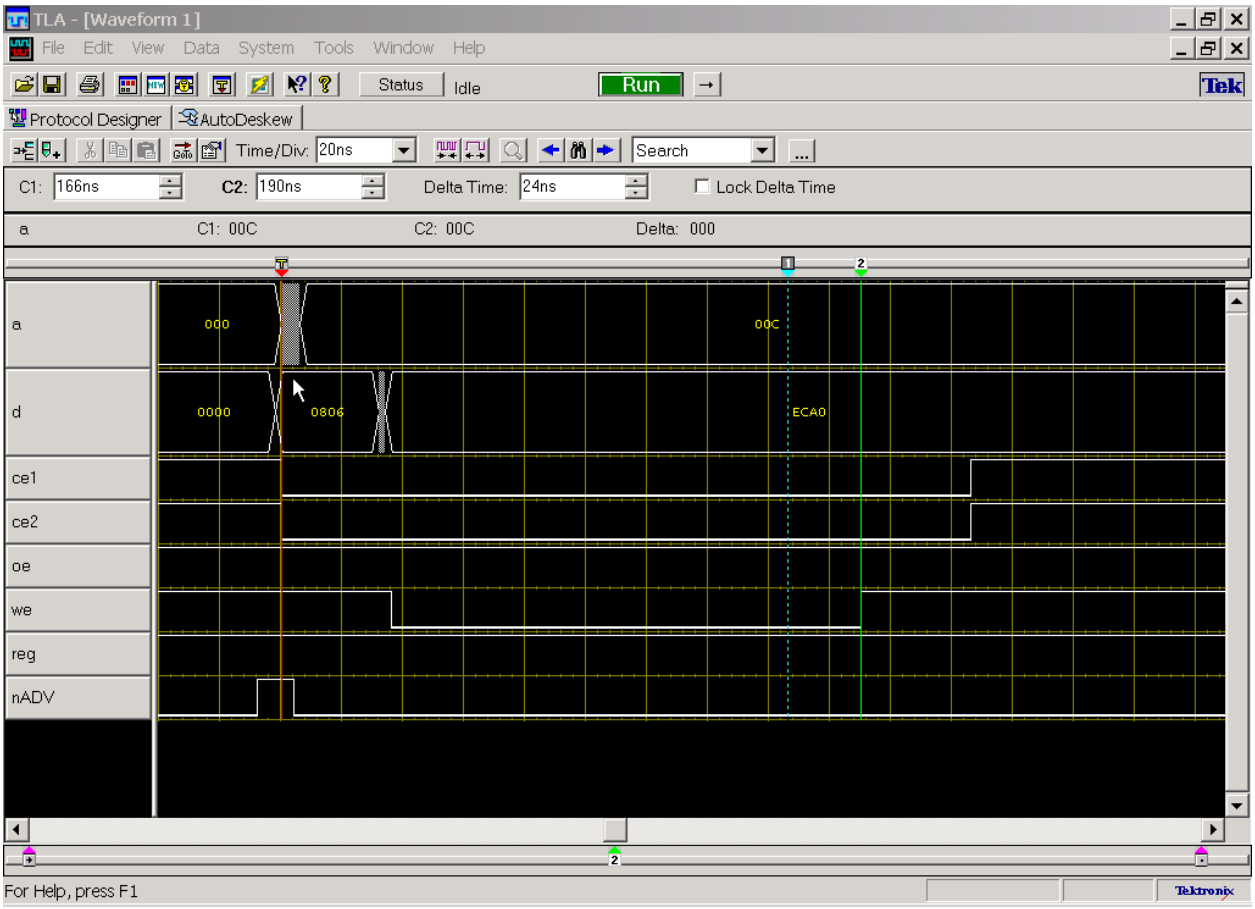


Figure 4.2: CompactFlash Write Timing

4.3 10/100 Ethernet PHY

The OMAP35x SOM-LV uses an SMSC LAN9221 Ethernet MAC+PHY to provide an easy-to-use networking interface. The four analog PHY interface signals (transmit/receive) each require an external impedance matching circuit to operate properly. Logic PD provides an example impedance matching circuit schematic in the *OMAP35x Development Kit Baseboard Schematic*. Note that the OMAP35x Development Kit Baseboard uses an Ethernet socket with integrated magnetics. Also, please note the TX+/- and RX+/- pairs must be routed as differential pairs on the baseboard PCB.

4.4 802.11 Wireless Ethernet

The OMAP35x SOM-LV uses a Murata LBEH19XMMC 802.11b/g/n + Bluetooth 2.1 Wireless IC to provide an easy-to-use wireless networking interface. The LBEH19XMMC is connected to the OMAP35x processor through SDIO3 and the connector is located on the PCB at reference designator J4.

NOTE: The Bluetooth interface on the LBEH19XMMC is not used. Please see Section 4.5 for Bluetooth on the OMAP35x SOM-LV.

4.5 Bluetooth

The OMAP35x SOM-LV uses a TI HPABT6300 BlueLink to provide a Bluetooth interface. The HPABT6300 is connected to the OMAP35x processor through McSPI1 and PCM. The connector is located on the PCB at reference designator J3.

4.6 Audio Codec

The OMAP35x processor has multiple Multi-channel Buffered Serial Port (McBSP) interfaces that support PCM and I2S formats. Both PCM and I2S serial paths drive the built-in TPS65950 audio codec. From the TPS65950, the outputs are CODEC_OUTL and CODEC_OUTR; these signals are available from the expansion connectors.

The codec in the TPS65950 performs up to full-duplex codec functions and supports variable sample rates from 8–96k samples per second. See the "Audio" chapter in TI's *TPS65950 OMAP Power Management and System Companion Device TRM* for more information.

NOTE: The OMAP35x SOM-LV also offers alternate serial interfaces for other codec devices. If you are looking for a different codec option, Logic PD has previously interfaced different high-performance audio codecs into other SOMs. Contact Logic PD for assistance in selecting an appropriate audio codec for your application.

4.7 Display Interface

The OMAP35x processor has a built-in LCD controller supporting STN, color STN, and TFT panels at a resolution of up to XGA 1024 x 768 x 24-bit color. See TI's *OMAP35x TRM* for further information on the integrated LCD controller. The signals from the OMAP35x LCD controller are organized by bit and color and can be interfaced through the expansion connectors. Logic PD has written drivers for panels of different types and sizes. Please contact Logic PD before selecting a panel for your application.

IMPORTANT NOTE: Using the internal graphics controller will affect processor performance. Selecting display resolutions and color bits per pixel will vary processor busload.

4.8 Serial Interfaces

The OMAP35x SOM-LV comes with the following serial channels: UARTA, UARTB, UARTC, SPI, and two I2C ports. If additional serial channels are required, please contact Logic PD for reference designs. Please see TI's *OMAP35x TRM* for further information regarding serial communications.

4.8.1 UARTA

UARTA has been configured as the main OMAP35x SOM-LV serial port based on the processor UART1. It is an asynchronous 16C750-compatible UART. This UART provides a high-speed serial interface that uses 64 byte First In / First Out (FIFO) and is capable of sending and receiving serial data simultaneously. The signals from the OMAP35x SOM-LV are 1.8V Transistor-Transistor Logic (TTL) level signals, not RS232 level signals. The end-product design must provide an external RS232 transceiver for RS232 applications. Logic PD has provided an example reference design with the *OMAP35x Development Kit Baseboard*

Schematic document. When choosing an RS232 transceiver, the designer should keep cost, availability, ESD protection, and data rates in mind.

The UARTA baud rate is set to a default 115.2 Kbits/sec, though it supports most common serial baud rates.

4.8.2 UARTB

Serial Port UARTB (processor UART3) is an asynchronous 16C750-compatible UART. This UART is a high-speed serial interface that uses FIFO and is capable of sending and receiving serial data simultaneously. The signals from the OMAP35x SOM-LV are TTL level signals, not RS232 level signals. The UARTB baud rate can also be set to most common serial baud rates.

4.8.3 UARTC

Serial port UARTC (processor UART2) is an asynchronous 16C750-compatible UART. This UART is a high-speed serial interface that uses FIFO and is capable of sending and receiving serial data simultaneously. The signals from the OMAP35x SOM-LV are TTL level signals, not RS232 level signals. The UARTC baud rate can also be set to most common serial baud rates.

4.8.4 McSPI

The OMAP35x SOM-LV provides an external SPI port with multiple chip selects.

4.8.5 I2C

The OMAP35x SOM-LV supports two dedicated external I2C ports. The clock and data signals for both ports have 4.7K pull-up resistors to their respective power rails on the SOM. Please see TI's *OMAP35x TRM* for further information.

4.8.5.1 Reserved I2C Addresses

The OMAP35x SOM-LV contains a product ID chip that connects to the I2C bus. Logic PD software uses this product ID chip to determine hardware version information. As a result, the 7-bit I2C addresses listed below are used by the product ID chip and must be avoided in custom designs:

- 101 1000
- 101 1001
- 101 1010
- 101 1011
- 101 1100
- 101 1101

4.9 USB Interface

The OMAP35x SOM-LV supports three USB 2.0 high-speed host ports and one USB 2.0 On-the-Go (OTG) port, which can function as a host or device/client. In order to for the port to operate as a host, a proper adapter cable must be used; Logic PD recommends one similar to

the USB adapter cable by Digi-Key[12] (part number 10-00003-ND). All ports can operate at up to 480 Mbit/sec. The processor has the USB controller internal to the OMAP for the OTG port; an external PHY built into the TPS65950 supports the OTG port.

The OMAP35x SOM-LV also has an external USB transceiver to support high-speed host. The external transceiver is an SMSC USB3320 that is connected through the USB2 ULPI interface of the OMAP35x microcontroller. The output of the USB3320 is routed to an SMSC USB2513 USB high-speed hub. The USB2513 is used to generate the three high-speed USB host ports that go off-board: USB2, USB4, and USB5. For more information on using both the USB host and OTG interfaces, please see TI's *OMAP35x TRM*.

IMPORTANT NOTE: In order to correctly implement USB on the OMAP35x SOM-LV, additional impedance matching circuitry may be required on the USBx_D+ and USBx_D- signals before they can be used. USB 2.0 requirements specify the signals must be routed as differential pairs with 90 ohm differential impedance. Refer to the *USB 2.0 Specification* for detailed information.

4.10 ADC/Touch Interface

The OMAP35x SOM-LV uses TI's TSC2004 Touch Screen Controller (TSC). The controller includes a 12-bit analog-to-digital converter (ADC). This TSC is used to support standard 4-wire resistive touch panels and one auxiliary A/D signal. The device is connected to the CPU by the OMAP I2C3 interface. Please see TI's *TSC2004 Datasheet* for more information.

4.11 General Purpose I/O

Logic PD designed the OMAP35x SOM-LV to be flexible and provide multiple options for analog and digital GPIO. There are numerous digital GPIO pins on the OMAP35X SOM-LV that interface to the OMAP35x processor and TPS65950 PMIC; please see Section 7 for more information. If certain peripherals are not desired, such as the LCD controller, chip selects, IRQs, or UARTs, more GPIO pins become available.

DESIGN NOTE: Due to buffer strength, an external serial resistor must be connected to the BGA balls where GPIO_120 through GPIO_129 are muxed with MMC signals. See "Section 24.2" in TI's *OMAP35x TRM* for additional information.

4.12 Onboard Logic Interfaces

The onboard logic interfaces are used to create additional functionality on the OMAP35x SOM-LV with the support of a few discrete logic components.

4.13 Expansion/Feature Options

The OMAP35x SOM-LV was designed for expansion and a variable feature set, providing all the necessary control signals and bus signals to expand the user's design. Some of these signals are buffered and brought out to the expansion connectors. It is possible for a user to expand the OMAP35x SOM-LV's functionality even further by adding host bus or ISA bus devices. Some features that are implemented on the OMAP35x processors but are not discussed herein

[12] http://www.digikey.com/scripts/DkSearch/dksus.dll?WT.z_header=search_go&lang=en&keywords=10-00003-ND&x=0&y=0&cur=USD

include: RTC, pulse width modulation (PWM), Secure Digital, MMC cards, SDIO cards, graphics accelerator, DSP codecs, Image Processing Unit, 1-wire interface, and the debug module. See TI's *OMAP35x TRM* and Logic PD's *OMAP35X SOM-LV Schematic* for more details.

Logic PD has experience implementing additional options, including other audio codecs, Ethernet ICs, co-processors, and components on SOMs. Please contact Logic PD for potential reference designs before selecting your peripherals.

DESIGN NOTE: The OMAP General Purpose Memory Controller (GPMC) bus is used by several peripherals on the OMAP35x SOM-LV. It is recommended that only one external device be connected to the GPMC bus. If more than one device is required, a buffer should be used.

DESIGN NOTE: Due to buffer strength, an external serial resistor must be connected to the BGA balls corresponding to any MMC/SD1 signal or alternate function on those same BGA balls. See "Section 24.2" in TI's *OMAP35x TRM* for additional information.

5 System Integration

5.1 Configuration

The OMAP35x SOM-LV was designed to meet multiple applications for users with specific design and budget requirements. As a result, this OMAP35x SOM-LV supports a variety of embedded operating systems and supports the following hardware configurations:

- Flexible memory footprint: 128 or 256 MB mobile DDR SDRAM
- Flexible NOR flash footprint: 0, 8, 16, or 32 MB NOR flash
- Flexible NAND flash footprint: 0, 256, or 512 MB
- Optional SMSC LAN9221 10/100 Ethernet PHY
- Optional Murata LBEH19XMMC 802.11b/g/n
- Optional TI BRF6300 Bluetooth

Please contact Logic PD for additional hardware configurations to meet your application needs.

5.2 Resets

The OMAP35x SOM-LV has a reset input (MSTR_nRST) and a reset output (RESET_nOUT/SYS_nRESWARM). External devices use MSTR_nRST to assert reset to the product. The OMAP35x SOM-LV uses RESET_nOUT to indicate to other devices that the SOM is in reset.

5.2.1 Master Reset (MSTR_nRST)—Reset Input

Logic PD suggests that custom designs implementing the OMAP35x SOM-LV use the MSTR_nRST signal as the "pin-hole" reset used in commercial embedded systems. The MSTR_nRST triggers a power-on-reset event to the OMAP35x processor and resets the entire CPU.

IMPORTANT NOTE: The MSTR_nRST does not reset the TPS65950 PMIC; the PMIC is only reset by removing power from the SOM. Any custom reset circuit design should guard the assertion of the reset lines during a low power state so as to prevent power-up in a low or bad power condition. (Powering up in a low or bad power condition will cause data corruption and, possibly, temporary system lockup). See Section 5.6 for further details. Either one of the following two conditions will cause a system-wide reset: power on the MSTR_nRST signal or a low pulse on the MSTR_nRST signal.

Low Pulse on MSTR_nRST Signal:

A low pulse on the MSTR_nRST signal, asserted by an external source (for example, the reset button on the custom design application) will bring MSTR_nRST low until the assertion source is de-asserted. There is no delay beyond the de-assertion of the external MSTR_nRST signal source, so the custom design must ensure that the assertion time is sufficient for all related peripherals.

Logic PD suggests that de-bouncing be used to generate a clean, one-shot reset signal for any external assertion source that triggers the MSTR_nRST signal, analog or digital.

5.2.2 OMAP35x SOM-LV Reset (RESET_nOUT/SYS_nRESWARM)—Reset output

All hardware peripherals should connect their hardware-reset pin to the RESET_nOUT (SYS_nRESWARM) signal on the expansion connector. Internally, all OMAP35x SOM-LV peripheral hardware reset pins are connected to the RESET_nOUT net.

If the output of the onboard voltage-monitoring circuit is asserted (active low), the user can expect to lose information stored in RAM. The data loss occurs because the CPU is reset to its reset defaults.

5.3 Interrupts

The OMAP35x processor incorporates the ARM Cortex-A8 interrupt controller, which provides many inter-system interrupt sources and destinations. Most external GPIO signals can also be configured as interrupt inputs by configuring their pin control registers. Logic PD BSPs set up and process all onboard system and external OMAP35X SOM-LV interrupt sources. Refer to TI's *OMAP35x TRM* for further information on using interrupts.

5.4 JTAG Debugger Interface

The JTAG connection on the OMAP35x SOM-LV allows recovery of corrupted flash memory, real-time application debug, and DSP development. There are several third-party JTAG debuggers available for TI microcontrollers. The following signals make up the JTAG interface to the OMAP35x processor: TDI, TMS, TCK, TDO, nTRST, RTCK, EMU0, EMU1, and MSTR_nRST (MSTR_nRST is only required for some JTAG tools; see the JTAG tool documentation for exact pinout). These signals should interface directly to a 20-pin 0.1" through-hole connector, as shown on the *OMAP35x Development Kit Baseboard Schematic*.

IMPORTANT NOTE: When laying out the 20-pin connector, realize that it may not be numbered as a standard 20-pin 0.1" insulation displacement connector (IDC) through-hole connector. See the OMAP35x Development Kit reference design for further details. Each JTAG tool vendor may define the 20-pin IDC connector pin-out differently.

5.5 ETM Adapter Interface

The Embedded Trace Macrocell (ETM) interface signals are available through connector J5 on the OMAP35x SOM-LV. Logic PD developed an adapter board, included with the OMAP35x Development Kit, that converts the available signals on J5 to the standard Mictor connector interface used by most common third-party ETM tool providers. The connector supports ETM_D[15:0], ETM_CLK, ETM_CTL, and the JTAG signals listed in Section 5.4.

IMPORTANT NOTE: The ETM interface will not operate at fastest speed due to multiplexed signals.

5.6 Power Management

5.6.1 System Power Supplies

In order to ensure a flexible design, the OMAP35x SOM-LV has the following power areas: MAIN_BATTERY, 5V, 3.3V, BACKUP_BATT. All power areas are inputs to the OMAP35x SOM-LV. The module also provides reference voltages to specific peripheral areas. Reference voltages are named VREF_xxxx on the expansion connectors. They are outputs from the OMAP35x SOM-LV and should only be used as reference voltage inputs to level shifting devices on baseboard designs.

IMPORTANT NOTE: If USB1_VBUS is powered externally it will power the SOM, even if MAIN_BATTERY is disconnected. Additionally, if U24 is populated, USB1_VBUS can charge MAIN_BATTERY. This functionality can be controlled by software. Please refer to the *TPS65950 TRM* for more information.

5.6.1.1 MAIN_BATTERY

The MAIN_BATTERY input is the main source of power for the OMAP35x SOM-LV. This input expects a voltage within typical single lithium-ion battery limits which generally operate from 2.8 V to 4.2 V. If a lithium-ion battery is not used as the main power source, it is recommended to supply a fixed 3.3 V supply. The TPS65950 power management controller takes the MAIN_BATTERY rail input and creates all onboard voltages. If the design is required to maintain RAM contents in a critical power situation (e.g., low battery, loss of power), the MAIN_BATTERY supply should be maintained above the minimum level at all costs (see Section 2). Logic PD suggests using standby mode to prepare the system for a critical power condition. In this way, the SDRAM is placed into self-refresh and the processor is placed into the standby state. (Please note the description of standby mode in Section 5.6.3.3 below.) The MAIN_BATTERY supply must stay within the acceptable levels specified in Section 2 unless experiencing power down or critical power conditions.

5.6.1.2 5V

The 5V input is not required for product operation. The 5V input is only used when the charge path components are populated on the OMAP35x SOM-LV. These optional charge path circuits allow in-system charging of a single cell lithium-ion battery source when a 5V power is applied to the 5V supply. Some designs will require a separate battery charging circuit on the baseboard to charge the main battery source. Charge current is limited to 1 Amp.

5.6.1.3 3.3V

The 3.3V rail is used to power a few legacy interfaces on the OMAP35x SOM-LV that require 3.3V. The baseboard should provide 3.3V to the OMAP35x SOM-LV when 10/100 Ethernet, USB host, or the ETM interface is required on the final product. Typically this can be implemented as a low dropout (LDO) or switching regulator connected to the MAIN_BATTERY power source on the baseboard. The 3.3V supply must stay within the acceptable levels specified in Section 2 unless experiencing power down or critical power conditions. Under critical power conditions, Logic PD suggests notifying the system through the assertion of a standby sequence first and then powering off this supply.

IMPORTANT NOTE: The 3.3V rail is required when Ethernet or USB are populated to prevent these devices from pulling the GPMC bus signals low or causing damage due to back power.

Ethernet and USB are populated on all standard configuration OMAP35x SOM-LVs; if a standard OMAP35x SOM-LV is used to test custom baseboard designs, there must be a method to apply 3.3V to the OMAP35x SOM-LV. This 3.3V circuitry can be removed after development if the production OMAP35x SOM-LV does not contain Ethernet or USB.

5.6.1.4 BACKUP_BATT

The BACKUP_BATT power rail is used to power the onboard TPS65950 PMIC, power management state machine, and RTC circuit when MAIN_BATTERY is not present. Always power this rail to maintain the clock and power state of the product. A lithium-ion coin cell typically supplies power to this rail. The TPS65950 PMIC overrides this input when MAIN_BATTERY is applied.

5.6.2 System Power Management

Good power management design is important in any system development and embedded system design is no exception. In embedded system design, power management is typically one of the most complicated areas due to the dramatic effect it has on product cost, performance, usability, and overall customer satisfaction. Many factors affect a power-efficient hardware design: power supply selection (efficiency), clocking design, IC and component selection, etc. The OMAP35x SOM-LV was designed with these aspects in mind while also providing maximum flexibility in software and system integration.

On the OMAP35x SOM-LV there are many different software configurations that drastically affect power consumption: microcontroller core clock frequency, bus clock frequency, peripheral clocks, bus modes, power management states; peripheral power states and modes; product user scenarios; interrupt handling; and display settings (resolution, backlight, refresh, bits per pixel, etc). These settings are typically initialized in the startup software routines and may be modified later in the operating system and application software. Information on these items can be found in the appropriate documents such as the *LogicLoader v2.4 User Manual* or the specific BSP manual.

5.6.3 Microcontroller

The OMAP35x processor's power management scheme was designed for the cellular handset market, so naturally the static and dynamic power consumption has very flexible controls allowing designers to tweak the processor to minimize end-product power consumption. Logic PD software BSPs take advantage of dynamic power switching (DPS) and SmartReflex adaptive voltage control (AVC) to maximize power savings.

5.6.3.1 Run State

Run is the normal operating state for the OMAP35x SOM-LV in which oscillator outputs and all clocks are hardware enabled. The OMAP35x SOM-LV can enter run mode from any state. A standby-to-run transition occurs on any valid wakeup event, such as the assertion or any enabled interrupt signal. All required power supplies are active in this state. Please see TI's *OMAP35xTRM* for further information.

5.6.3.2 Suspend State

Suspend is the hardware power-down state for the OMAP35x SOM-LV, allowing for lower power consumption. The suspend state is designed to reduce power consumption while the OMAP35x SOM-LV is waiting for an event, such as a keyboard input. In Logic PD BSPs, the suspend state is entered by asserting the nSUSPEND signal or through software commands. All power supplies remain active and system context is retained. An internal or external wakeup event can cause the processor to transition back to run mode. Please see TI's *OMAP35x TRM* for further information.

5.6.3.3 Standby State

Standby is the lowest power state for the OMAP35x SOM-LV. This state is entered in Logic PD BSPs by asserting the nSTANDBY signal or through software commands. The OMAP35x processor is put into the lowest power state and all clocks are stopped. The MAIN_BATTERY power rail should be maintained if the low-power DDR SDRAM contents wish to be retained. Internal or external wakeup events can cause a return to the run state.

5.7 ESD Considerations

The OMAP35x SOM-LV was designed to interface to a customer's peripheral board, while remaining low cost and adaptable to many different applications. The OMAP35x SOM-LV does not provide any onboard ESD protection circuitry—this must be provided by the product in which it is used. Logic PD has extensive experience in designing products with ESD requirements. Please contact Logic PD if you need any assistance in ESD design considerations.

6 Memory & I/O Mapping

On the OMAP35x microcontroller, all address mapping for the GPMC chip select signals is listed below. Mapped chip select signals for the processor are available as outputs from the microcontroller and are assigned as described in Table 6.1 below.

Table 6.1: Chip Select Signals

Chip Select	Device/Feature	Notes
nCS0	POP NAND / boot NOR	Boot chip select for POP NAND device or external NOR when POP does not include NAND
nCS1	10/100 Ethernet	SMSC LAN9221
nCS2	ON-/OFF-board NOR	Micron Parallel NOR Flash Embedded Memory
nCS3	External Memory Mode CompactFlash	
nCS4	External nCS_A	Available for use by an off-board external device
nCS5	External nCS_B	Available for use by an off-board external device

NOTE: Memory addresses for chip selects on the OMAP35x SOM-LV are configurable by software; therefore, precise address locations cannot be provided. Please consult the *LogicLoader v2.4 User Manual* and the *OMAP35x SOM-LV LogicLoader User Manual Addendum* for memory map information.

7 Pin Descriptions and Functions

IMPORTANT NOTE: The following pin descriptions and states are provided for the default pin usage. Many of the signals defined in the tables below can be configured as input or outputs—most GPIOs on the OMAP35x processor can be configured as either inputs or outputs—and have different functions. It is critical to review all signals in the final design (both electrical and software) to verify the necessary configuration (external pull-ups/pull-downs).

IMPORTANT NOTE: Please pay attention to the reference voltage used to power each signal in the table below, especially when used as a GPIO. Not all power rails coming out of the TPS65950 PMIC are turned on by default and may need to be enabled by software. Reference voltages for OMAP35x processor signals can be found in TI's *OMAP3530/25 Applications Processor Datasheet*.

NOTE: When two signal names are provided, the signals in parentheses are the net names specific to OMAP35x SOM-LV; the non-parenthetical names are the signal names that are general to the SOM-LV form factor.

7.1 J1 Connector 240-Pin Descriptions

J1 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J1.1	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.2	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.3	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.4	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.5	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.6	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.7	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.8	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.9	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.10	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.11	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J1.12	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.

J1 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J1.13	uP_nWAKEUP	A11(PMIC)	PWRON(PMIC)	I	Max 4.3V (MAIN_BATTERY)	Active low. Software can use this signal as an interrupt to transition to RUN state from lower power states. Software is required for proper operation. This signal has a 4.75K pull-up.
J1.14	ETHER_TX+	—	—	O	3.3V	This output pair drives 10/100 Mb/s data to the transmit lines. Route as differential pair with ETHER_TX-. Requires external magnetics. See example LV-Baseboard design for reference components.
J1.15	nSUSPEND	W21	McBSP1_CLKX/ McBSP3_CLKX/ GPIO_162	I	1.8V	Software can use this signal to enter low power states from RUN mode. Software is required for correct operation.
J1.16	ETHER_TX-	—	—	O	3.3V	This output pair drives 10/100 Mb/s data to the transmit lines. Route as differential pair with ETHER_TX+. Requires external magnetics. See example LV-Baseboard design for reference components.
J1.17	nSTANDBY	K26	McBSP1_FSX/ McSPI4_CS0/ McBSP_FSX/ GPIO_161	I	1.8V	Software can use this signal to enter low power states from RUN mode. Software is required for correct operation.
J1.18	ETHER_RX+	—	—	I	3.3V	This input pair receives 10/100 Mb/s data from the receive lines. Route as differential pair with ETHER_RX-. Requires external magnetics. See example LV-Baseboard design for reference components.
J1.19	USB1_ID	R11(PMIC)	ID (PMIC)	I/O	5.0V	Tie to pin four of a USB 2.0 OTG compliant connector. This signal negotiates host/device operation with an external USB product. See example LV-Baseboard design for reference components.
J1.20	ETHER_RX-	—	—	I	3.3V	This input pair receives 10/100 Mb/s data from the receive lines. Route as differential pair with ETHER_RX+. Requires external magnetics. See example LV-Baseboard design for reference components.
J1.21	USB1_VBUS	(See Schematic)	(See Schematic)	I/O	5.0V (See note 2)	Ties to pin one of a USB 2.0 OTG compliant connector. This signal indicates to the USB controller that an external USB Host has been connected or can provide power to USB Device peripherals. See example LV-Baseboard design for reference components.

J1 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J1.22	ACT_nLNK_LED /LAN_LED2	—	—	O	3.3V	Active low. Asserts when there is valid Ethernet connection. Deasserts during Ethernet traffic indicating activity. See example LV-Baseboard design for reference components.
J1.23	USB1_nOC	V21	McBSP1_DX/ McSPI4_SIMO/ McBSP3_DX/ GPIO_158	I	1.8V	Active low. USB OTG over current flag. Indicates to PHY an over current condition exists on the USB OTG port when an external USB power switch is used. If TPS65950 charge pump is used, this signal may be used as a GPIO. This signal has a 10k pull-down resistor on the OMAP35x SOM-LV.
J1.24	SPD_LED_n100 M_10M/LAN_LE D1	—	—	O	3.3V	Active low. Asserts to indicate operation speed, either 10Mbs (high) or 100Mbs (low) connection. See example LV-Baseboard design for reference components.
J1.25	USB1_PWR_nE N	G11(PMIC)	GPIO.13/ LEDSYNC (PMIC)	O	1.8V	Active low. USB OTG power enable. Enables power to the external USB power switch if used. If TPS65950 charge pump is used, this signal may be used as a GPIO.
J1.26	VREF_ETHERNE T (3.3V_A)	(See Schematic)	(See Schematic)	O	3.3V	Output from the OMAP35x SOM-LV that drives the impedance network and magnetics. Specific to Ethernet PHY requirements. See example LV-Baseboard design for reference components.
J1.27	USB1_D+	T10(PMIC)	DP/UART3.RXD (PMIC)	I/O	Variable (See note 1)	USB OTG port 1 I/O data plus signal. Route as differential pair with USB1_D-. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differential impedance.
J1.28	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.29	USB1_D-	T11(PMIC)	DN/UART3.TXD (PMIC)	I/O	Variable (See note 1)	USB OTG port 1 I/O data minus signal. Route as differential pair with USB1_D+. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differential impedance.
J1.30	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.31	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J1.32	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J1.33	USB2_D+	—	—	I/O	Variable (See note 1)	USB Host port 2 I/O data plus signal. Route as differential pair with USB2_D-. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differential impedance.
J1.34	uP_GPIO_7	L4 (PMIC)	GPIO.2/ HSDET/TEST1 (PMIC)	I/O	1.8V	TPS65950 GPIO available to user. Connected to TPS65950 GPIO.2.

J1 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J1.35	USB2_D-	—	—	I/O	Variable (See note 1)	USB Host port 2 I/O data minus signal. Route as differential pair with USB2_D+. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differential impedance.
J1.36	uP_GPIO_6	P13(PMIC)	GPIO.15/TEST2 (PMIC)	I/O	1.8V	TPS65950 GPIO available to user. Connected to TPS65950 GPIO.15.
J1.37	USB2_nOC	—	—	I	3.3V (5V tolerant)	Active low. USB Host over current flag. Indicates to PHY an over current condition exists on the USB Host port.
J1.38	uP_GPIO_5	N14(PMIC)	GPIO.7/ VIBRA.SYNC/ PWM1/TEST4 (PMIC)	I/O	1.8V	TPS65950 GPIO available to user. Connected to TPS65950 GPIO.7.
J1.39	USB2_PWR_nEN	—	—	O	3.3V	Active low. USB Host power enable. Enables power to the external USB power switch. This signal has a 10k pull-up to 3.3V. See example LV-Baseboard design for reference components.
J1.40	uP_D0	K1	GPMC_D0	I/O	1.8V	Processor GPMC bus data bit 0. (See notes 3 & 4)
J1.41	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.42	uP_D1	L1	GPMC_D1	I/O	1.8V	Processor GPMC bus data bit 1. (See notes 3 & 4)
J1.43	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.44	uP_D2	L2	GPMC_D2	I/O	1.8V	Processor GPMC bus data bit 2. (See notes 3 & 4)
J1.45	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.46	uP_D3	P2	GPMC_D3	I/O	1.8V	Processor GPMC bus data bit 3. (See notes 3 & 4)
J1.47	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.48	uP_D4	T1	GPMC_D4	I/O	1.8V	Processor GPMC bus data bit 4. (See notes 3 & 4)
J1.49	3.3V_nEN (DGND)	—	—	O	1.8V	3.3V external enable pin. Active low, signals to the baseboard the 3.3V supply should be enabled.
J1.50	uP_D5	V1	GPMC_D5	I/O	1.8V	Processor GPMC bus data bit 5. (See notes 3 & 4)
J1.51	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J1.52	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J1.53	A0 (DGND)	—	—	O	1.8V	Processor GPMC bus address bit 0.
J1.54	uP_D6	V2	GPMC_D6	I/O	1.8V	Processor GPMC bus data bit 6. (See notes 3 & 4)

J1 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J1.55	A1 (uP_LA1)	—	—	O	1.8V	Latched Processor GPMC bus address bit 1.
J1.56	uP_D7	W2	GPMC_D7	I/O	1.8V	Processor GPMC bus data bit 7. (See notes 3 & 4)
J1.57	A2 (uP_LA2)	—	—	O	1.8V	Latched Processor GPMC bus address bit 2.
J1.58	uP_D8	H2	GPMC_D8/ GPIO_44	I/O	1.8V	Processor GPMC bus data bit 8. (See notes 3 & 4)
J1.59	A3 (uP_LA3)	—	—	O	1.8V	Latched Processor GPMC bus address bit 3.
J1.60	uP_D9	K2	GPMC_D9/ GPIO_45	I/O	1.8V	Processor GPMC bus data bit 9. (See notes 3 & 4)
J1.61	A4 (uP_LA4)	—	—	O	1.8V	Latched Processor GPMC bus address bit 4.
J1.62	uP_D10	P1	GPMC_D10/ GPIO_46	I/O	1.8V	Processor GPMC bus data bit 10. (See notes 3 & 4)
63	A5 (uP_LA5)	—	—	O	1.8V	Latched Processor GPMC bus address bit 5.
J1.64	uP_D11	R1	GPMC_D11/ GPIO_47	I/O	1.8V	Processor GPMC bus data bit 11. (See notes 3 & 4)
J1.65	A6 (uP_LA6)	—	—	O	1.8V	Latched Processor GPMC bus address bit 6.
J1.66	uP_D12	R2	GPMC_D12/ GPIO_48	I/O	1.8V	Processor GPMC bus data bit 12. (See notes 3 & 4)
J1.67	A7 (uP_LA7)	—	—	O	1.8V	Latched Processor GPMC bus address bit 7.
J1.68	uP_D13	T2	GPMC_D13/ GPIO_49	I/O	1.8V	Processor GPMC bus data bit 13. (See notes 3 & 4)
J1.69	A8 (uP_LA8)	—	—	O	1.8V	Latched Processor GPMC bus address bit 8.
J1.70	uP_D14	W1	GPMC_D14/ GPIO_50	I/O	1.8V	Processor GPMC bus data bit 14. (See notes 3 & 4)
J1.71	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J1.72	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J1.73	A9 (uP_LA9)	—	—	O	1.8V	Latched Processor GPMC bus address bit 9.
J1.74	uP_D15	Y1	GPMC_D15/ GPIO_51	I/O	1.8V	Processor GPMC bus data bit 15. (See notes 3 & 4)
J1.75	A10 (uP_LA10)	—	—	O	1.8V	Latched Processor GPMC bus address bit 10.
J1.76	D16 (RFU)	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.77	A11 (uP_LA11)	—	—	O	1.8V	Latched Processor GPMC bus address bit 11.
J1.78	D17 (RFU)	—	—	I/O	NA	Reserved for future use. Do not connect.

J1 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J1.79	A12 (uP_LA12)	—	—	O	1.8V	Latched Processor GPMC bus address bit 12. This signal is also connected to J2.44.
J1.80	D18 (RFU)	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.81	A13 (uP_LA13)	—	—	O	1.8V	Latched Processor GPMC bus address bit 13.
J1.82	D19 (RFU)	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.83	A14 (uP_LA14)	—	—	O	1.8V	Latched Processor GPMC bus address bit 14.
J1.84	D20 (RFU)	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.85	A15 (uP_LA15)	—	—	O	1.8V	Latched Processor GPMC bus address bit 15.
J1.86	D21 (RFU)	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.87	A16 (uP_LA16)	—	—	O	1.8V	Latched Processor GPMC bus address bit 16.
J1.88	D22 (RFU)	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.89	A17 (uP_A1)	N4	GPMC_A1/ GPIO_34	O	1.8V	Processor GPMC bus address bit 17. (See note 3)
J1.90	D23 (RFU)	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.91	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J1.92	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J1.93	A18 (uP_A2)	M4	GPMC_A2/ GPIO_35	O	1.8V	Processor GPMC bus address bit 18. (See note 3)
J1.94	D24 (RFU)	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.95	A19 (uP_A3)	L4	GPMC_A3/ GPIO_36	O	1.8V	Processor GPMC bus address bit 19. (See note 3)
J1.96	D25 (RFU)	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.97	A20 (uP_A4)	K4	GPMC_A4/ GPIO_37	O	1.8V	Processor GPMC bus address bit 20. (See note 3)
J1.98	D26 (RFU)	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.99	A21 (uP_A5)	T3	GPMC_A5/ GPIO_38	O	1.8V	Processor GPMC bus address bit 21. (See note 3)
J1.100	D27 (RFU)	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.101	A22 (uP_A6)	R3	GPMC_A6/ GPIO_39	O	1.8V	Processor GPMC bus address bit 22. (See note 3)
J1.102	D28 (RFU)	—	—	I/O	NA	Reserved for future use. Do not connect.

J1 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J1.103	A23 (uP_A7)	N3	GPMC_A7/ GPIO_40	O	1.8V	Processor GPMC bus address bit 23. (See note 3)
J1.104	D29 (RFU)	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.105	A24 (uP_A8)	M3	GPMC_A8/ GPIO_41	O	1.8V	Processor GPMC bus address bit 24. (See note 3)
J1.106	D30 (RFU)	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.107	A25 (uP_A9)	L3	GPMC_A9/ SYS_nDMAREQ2/GPIO_42	O	1.8V	Processor GPMC bus address bit 25. (See note 3)
J1.108	D31 (RFU)	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.109	uP_nWAIT	L8	GPMC_WAIT1/ GPIO_63	I	1.8V	Active low. Processor bus GPMC_WAIT1 signal. Used to extend bus transactions beyond programmed wait states. The external device signals completion of the cycle by deasserting the uP_nWAIT signal. This signal has a 1K pull-up. (See note 3)
J1.110	VREF_DATA_BUS (VIO_1V8)	(See Schematic)	(See Schematic)	O	1.8V	Voltage reference output created on OMAP35x SOM-LV for the data bus.
J1.111	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J1.112	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J1.113	uP_nIRQD (CSI_D11)	C26	CAM_D11/ GPIO_110	I	1.8V	Active low. Software can use as a hardware interrupt. **NOTE:** This signal is used as card detect on the Zoom OMAP35x Development Kit and is recognized as such by Logic PD software. If using the OMAP35x SOM-LV on a custom baseboard that uses an SD card socket without card detect, this signal must be grounded.
J1.114	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.115	uP_nIRQC	D25	CAM_STROBE/ GPIO_126	I	1.8V	Active low. Software can use as a hardware interrupt. **NOTE:** This is also designated as a SD write protection signal when SD is used; therefore, this signal must be left floating and not grounded to prevent any possible issues.
J1.116	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.117	uP_nIRQB	B23	CAM_WEN/ CAM_SHUTTER/ GPIO_167	I	1.8V	Active low. Software can use as a hardware interrupt.
J1.118	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.

J1 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J1.119	uP_nIRQA	C23	CAM_FLD/ CAM_GLOBAL_ RESET/ GPIO_98	I	1.8V	Active low. Software can use as a hardware interrupt.
J1.120	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.121	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.122	uP_UARTC_CTS	AB26	UART2_CTS/ MCBSP3_DX/ GPT9_PWM_EVT/ GPIO_144	I	1.8V	Clear To Send signal for UART2.
J1.123	BUFF_DIR_DAT A	N8	GPMC_nCS7/ GPMC_IODIR/ McBSP4_FSX/ GPT8_PWM_EVT/ GPIO_58 (connected through an inverter)	O	1.8V	When low, external buffers should drive data from external devices towards the OMAP35x SOM-LV. (SOM-LV is reading). When high, external buffers should drive data from the OMAP35x SOM-LV towards external devices. (SOM-LV is writing).
J1.124	uP_UARTC_RTS	AB25	UART2_RTS/ MCBSP3_DR/ GPT10_PWM_EVT/ GPIO_145	O	1.8V	Ready To Send signal for UART2.
J1.125	uP_nOE	G2	GPMC_nOE	O	1.8V	Active low. Used to indicate processor is reading from external devices. This signal is also connected to J2.14.(See notes 3 & 4)
J1.126	uP_UARTC_RX	AD25	UART2_RX/ MCBSP3_FSX/ GPT8_PWM_EVT/ GPIO_147	I	1.8V	Serial Data Receive signal for UART2.
J1.127	uP_nWE	F4	GPMC_nWE	O	1.8V	Low indicates processor is writing. High indicates processor is reading. This signal also connects to J2.40. (See notes 3 & 4)
J1.128	uP_UARTC_TX	AA25	UART2_TX/ MCBSP3_CLKX/ GPT11_PWM_EVT/ GPIO_146	O	1.8V	Serial Data Transmit signal for UART2.
J1.129	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J1.130	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J1.131	uP_BUS_CLK	T4	GPMC_CLK/ GPIO_59	O	1.8V	Processor bus clock. Frequency varies based on software setup. **NOTE**: uP_BUS_CLK is only active on bus transactions, it does not run continuously. See TI's *OMAP35x Technical Reference Manual* and *Data Sheet* for additional information. **NOTE**: This signal may be shared with the PoP memory depending on the population.

J1 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J1.132	uP_UARTB_RX	H20	UART3_RX_IRRX/ GPIO_165	I	1.8V	Serial Data Receive signal for UART3.
J1.133	uP_DREQ0	AG11 J8	POP_INT0_FT GPMC_WAIT3/ SYS_nDMAREQ1/ GPIO_65	I	1.8V	DMA Request signal for DMA4. Connected to SYS_nDMAREQ1 of the OMAP35x. **NOTE:** This signal is shared with the POP NAND chip's LOCK pin. This signal should be left floating at power-on to avoid conflict. (See note 4)
J1.134	uP_UARTB_TX	H21	UART3_TX_IRTX/ GPIO_166	O	1.8V	Serial Data Transmit signal for UART3.
J1.135	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.136	uP_UARTB_CTS	H18	UART3_CTS_ RCTX/GPIO_163	I	1.8V	Clear To Send signal for UART3.
J1.137	uP_nBE0	G3	GPMC_nBE0_CLE/G PIO_60	O	1.8V	Processor bus Byte Lane Enable 0 bits [7:0] (See notes 3 & 4)
J1.138	uP_UARTB_RTS	H19	UART3_RTS_SD/ GPIO_164	O	1.8V	Ready To Send signal for UART3.
J1.139	uP_nBE1	U3	GPMC_nBE1/ GPIO_61	O	1.8V	Processor bus Byte Lane Enable 1 bits [15:8]
J1.140	uP_GPO_4	P12(PMIC)	GPIO.0/CD1/ JTAG.TDO (PMIC)	I/O	1.8V	TPS65950 GPIO available to user. Connected to TPS65950 GPIO.0. This signal has a 4.7K pull-down resistor.
J1.141	uP_nCS_B_EXT (nCS5)	R8	GPMC_nCS5/ SYS_nDMAREQ2/ McBSP4_DR/ GPT10_PWM_EVT/ GPIO_56	O	1.8V	External Chip select available for customer use. Also connected to J1.145.
J1.142	uP_GPIO_3	B26	CAM_XCLKB/ GPIO_111	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_111.
J1.143	uP_nCS_A_EXT (nCS4)	T8	GPMC_nCS4/ SYS_nDMAREQ1/ McBSP4_CLKX/ GPT9_PWM_EVT/ GPIO_55	O	1.8V	External Chip select available for customer use. Also connected to J1.147.
J1.144	VREF_I2C2 (VIO_1V8)	(See Schematic)	(See Schematic)	O	1.8V	Reference voltage output for I2C DATA and CLK signals.
J1.145	SLOW_nCS (uP_nCS_B_EX T/nCS5)	R8	GPMC_nCS5/ SYS_nDMAREQ2/ McBSP4_DR/ GPT10_PWM_EVT/ GPIO_56	O	1.8V	External Chip select available for customer use. Also connected to J1.141.
J1.146	uP_I2C2_SDA	AE15	I2C2_SDA/GPIO_1 8	I/O	1.8V	I2C channel 2 data signal. This signal has a 4.7K pull-up to the reference voltage onboard.
J1.147	FAST_nCS (uP_nCS_A_EX T/nCS4)	T8	GPMC_nCS4/ SYS_nDMAREQ1/ McBSP4_CLKX/ GPT9_PWM_EVT/ GPIO_55	O	1.8V	External Chip select available for customer use. Also connected to J1.143.

J1 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J1.148	uP_I2C2_SCL	AF15	I2C2_SCL/GPIO_168	I/O	1.8V	I2C channel 2 clock signal. This signal has a 4.7K pull-up to the reference voltage onboard.
J1.149	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J1.150	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J1.151	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.152	VREF_UARTA (VIO_1V8)	(See Schematic)	(See Schematic)	O	1.8V	Voltage reference output for UARTA signals.
J1.153	LCD_DON (ICT_JTAG_TMS)	N12 (PMIC)	GPIO.1/CD2/ JTAG.TMS (PMIC)	O	1.8V	LCD Data On signal.
J1.154	uP_UARTA_DSR	U21	McBSP1_DR/ McSPI4_SOMI/ McBSP3_DR/ GPIO_159	I	1.8V	Data Set Ready signal for UART1.
J1.155	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.156	uP_UARTA_DTR	AE21	SYS_BOOT5/ MMC2_DIR_DAT3/ GPIO_7	O	1.8V	Data Terminal Ready signal for UART1.
J1.157	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.158	uP_UARTA_RX	Y8	UART1_RX/ MCBSP1_CLKR/ MCSPI4_CLK/ GPIO_151	I	1.8V	Data Receive signal for UART1.
J1.159	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.160	uP_UARTA_TX	AA8	UART1_TX/ SSI1_DAT_TX/ GPIO_148	O	1.8V	Data Transmit signal for UART1.
J1.161	LCD_PANEL_PWR	AC1	McBSP4_FSX/ SSI1_WAKE/ HSUSB3_TLL_ DATA3/ MM3_TXEN_n/ GPIO_155	O	1.8V	LCD Panel Power signal.
J1.162	uP_UARTA_CTS	W8	UART1_CTS/ SSI1_RDY_TX/ HSUSB3_TLL_ CLK/GPIO_150	I	1.8V	Clear To Send signal for UART1.
J1.163	LCD_BACKLIGHT_PWR	AF21	SYS_BOOT6/ GPIO_8 (through Q3)	O	1.8V	LCD Backlight Power signal. Active High. This signal has a 10K pull-down resistor.
J1.164	uP_UARTA_RTS	AA9	UART1_RTS/ SSI1_FLAG_TX/ GPIO_149	O	1.8V	Ready To Send signal for UART1.
J1.165	LCD_HSYNC	D26	DSS_HSYNC/ GPIO_67	O	1.8V	LCD Horizontal Sync signal.

J1 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J1.166	uP_GPIO_2	AA10	JTAG_EMU1/ GPIO_31	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_31. This signal is also connected to J2.152.
J1.167	LCD_VSYNC	D27	DSS_VSYNC/ GPIO_68	O	1.8V	LCD Vertical Sync Signal.
J1.168	PWM0	M4 (PMIC)	GPIO.6/MUTE/ PWM0/TEST3 (PMIC)	O	1.8V	PWM output 0.
J1.169	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J1.170	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J1.171	LCD_DCLK	D28	DSS_PCLK/ GPIO_66	O	1.8V	LCD Data Clock output.
J1.172	BACKUP_BATT	M14	BKBAT	I	1.8V-3.3V	External input that supplies power to the onboard power management controller and RTC interface. This signal should be powered by a coin-cell type battery or an always-on power source.
J1.173	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.174	5V	(See Schematic)	(See Schematic)	I	4.8V-7V	5V power input. Used by power management controller to charge external MAIN_BATTERY supply.
J1.175	LCD_MDISP	E27	DSS_ACBIAS/ GPIO_69	O	1.8V	LCD MDISP signal.
J1.176	5V	(See Schematic)	(See Schematic)	I	4.8V-7V	5V power input. Used by power management controller to charge external MAIN_BATTERY supply.
J1.177	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.178	5V	(See Schematic)	(See Schematic)	I	4.8V-7V	5V power input. Used by power management controller to charge external MAIN_BATTERY supply.
J1.179	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.180	3.3V	(See Schematic)	(See Schematic)	I	3.3V	External 3.3V power input. This signal supplies power to 3.3V components onboard.
J1.181	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.182	3.3V	(See Schematic)	(See Schematic)	I	3.3V	External 3.3V power input. This signal supplies power to 3.3V components onboard.
J1.183	LCD_VREF (VPLL2)	(See Schematic)	(See Schematic)	O	1.8V	Voltage reference output for the LCD interface.
J1.184	3.3V	(See Schematic)	(See Schematic)	I	3.3V	External 3.3V power input. This signal supplies power to 3.3V components onboard.

J1 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J1.185	R1 (LCD_D11)	AD27	DSS_D11/ SDI_DAT1P/ GPIO_81	O	1.8V	LCD R1 data bit when operating in 16 bpp 5:6:5 color mode. Please reference the *OMAP35x TRM* for 24-bit LCD bus mapping.
J1.186	TOUCH_LEFT	—	—	I	max 3.1V	Touch panel LEFT input signal.
J1.187	R2 (LCD_D12)	AB28	DSS_D12/ SDI_DAT2N/ GPIO_82	O	1.8V	LCD R2 data bit when operating in 16 bpp 5:6:5 color mode. Please reference the *OMAP35x TRM* for 24-bit LCD bus mapping.
J1.188	TOUCH_RIGHT	—	—	I	max 3.1V	Touch panel RIGHT input signal.
J1.189	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J1.190	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J1.191	R3 (LCD_D13)	AB27	DSS_D13/ SDI_DAT2P/ GPIO_83	O	1.8V	LCD R3 data bit when operating in 16 bpp 5:6:5 color mode. Please reference the *OMAP35x TRM* for 24-bit LCD bus mapping.
J1.192	TOUCH_BOTTOM	—	—	I	max 3.1V	Touch panel BOTTOM input signal.
J1.193	R4 (LCD_D14)	AA28	DSS_D14/ SDI_DAT3N/ GPIO_84	O	1.8V	LCD R4 data bit when operating in 16 bpp 5:6:5 color mode. Please reference the *OMAP35x TRM* for 24-bit LCD bus mapping.
J1.194	TOUCH_TOP	—	—	I	max 3.1V	Touch panel TOP input signal.
J1.195	R5 (LCD_D15)	AA27	DSS_D15/ SDI_DAT3P/ GPIO_85	O	1.8V	LCD R5 data bit when operating in 16 bpp 5:6:5 color mode. Please reference the *OMAP35x TRM* for 24-bit LCD bus mapping.
J1.196	A/D4	N11(PMIC)	ADCIN5 (PMIC)	I	max 2.7V	Analog to digital converter input. Connected to TPS65950 ADCIN5. When not used, leave floating.
J1.197	G0 (LCD_D5)	AH24	DSS_D5/ UART3_TX_IRTX/ DY2/GPIO_75	O	1.8V	LCD G0 data bit when operating in 16 bpp 5:6:5 color mode. Please reference the *OMAP35x TRM* for 24-bit LCD bus mapping.
J1.198	A/D3	N8 (PMIC)	ADCIN4 (PMIC)	I	max 2.7V	Analog to digital converter input. Connected to TPS65950 ADCIN4. When not used, connect 100nF CAP to DGND.
J1.199	G1 (LCD_D6)	E26	DSS_D6/ UART1_TX/ GPIO_76	O	1.8V	LCD G1 data bit when operating in 16 bpp 5:6:5 color mode. Please reference the *OMAP35x TRM* for 24-bit LCD bus mapping.
J1.200	A/D2	P11(PMIC)	ADCIN3 (PMIC)	I	max 2.7V	Analog to digital converter input. Connected to TPS65950 ADCIN3. When not used, connect to DGND.
J1.201	G2 (LCD_D7)	F28	DSS_D7/ UART1_RX/ GPIO_77	O	1.8V	LCD G2 data bit when operating in 16 bpp 5:6:5 color mode. Please reference the *OMAP35x TRM* for 24-bit LCD bus mapping.

J1 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J1.202	A/D1	—	—	I	max 3.1V	Analog to digital converter input. Connected to Touch chip's AUX input. When not used, connect 100nF CAP to DGND.
J1.203	G3 (LCD_D8)	F27	DSS_D8/GPIO_78	O	1.8V	LCD G3 data bit when operating in 16 bpp 5:6:5 color mode. Please reference the *OMAP35x TRM* for 24-bit LCD bus mapping.
J1.204	MAIN_BATTERY	(See Schematic)	(See Schematic)	I	max 4.3V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed regulated power source.
J1.205	G4 (LCD_D9)	G26	DSS_D9/GPIO_79	O	1.8V	LCD G4 data bit when operating in 16 bpp 5:6:5 color mode. Please reference the *OMAP35x TRM* for 24-bit LCD bus mapping.
J1.206	MAIN_BATTERY	(See Schematic)	(See Schematic)	I	max 4.3V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed regulated power source.
J1.207	G5 (LCD_D10)	AD28	DSS_D10/ SDI_DAT1N/ GPIO_80	O	1.8V	LCD G5 data bit when operating in 16 bpp 5:6:5 color mode. Please reference the *OMAP35x TRM* for 24-bit LCD bus mapping.
J1.208	MAIN_BATTERY	(See Schematic)	(See Schematic)	I	max 4.3V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed regulated power source.
J1.209	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J1.210	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J1.211	B1 (LCD_D0)	AG22	DSS_D0/ UART1_CTS/DX0/GPIO_70	O	1.8V	LCD B1 data bit when operating in 16 bpp 5:6:5 color mode. Please reference the *OMAP35x TRM* for 24-bit LCD bus mapping.
J1.212	MAIN_BATTERY	(See Schematic)	(See Schematic)	I	max 4.3V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed regulated power source.
J1.213	B2 (LCD_D1)	AH22	DSS_D1/ UART1_RTS/DY0/GPIO_71	O	1.8V	LCD B2 data bit when operating in 16 bpp 5:6:5 color mode. Please reference the *OMAP35x TRM* for 24-bit LCD bus mapping.
J1.214	MAIN_BATTERY	(See Schematic)	(See Schematic)	I	max 4.3V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed regulated power source.
J1.215	B3 (LCD_D2)	AG23	DSS_D2/DX1/ GPIO_72	O	1.8V	LCD B3 data bit when operating in 16 bpp 5:6:5 color mode. Please reference the *OMAP35x TRM* for 24-bit LCD bus mapping.
J1.216	uP_GPIO_1	AA11	JTAG_EMU0/ GPIO_11	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_11. This signal is also connected to J2.154.

J1 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J1.217	B4 (LCD_D3)	AH23	DSS_D3/DY1/ GPIO_73	O	1.8V	LCD B4 data bit when operating in 16 bpp 5:6:5 color mode. Please reference the *OMAP35x TRM* for 24-bit LCD bus mapping.
J1.218	uP_GPIO_0	AH4	MMC2_DAT1/ GPIO_133	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_133.
J1.219	B5 (LCD_D4)	AG24	DSS_D4/ UART3_RX_IRRX/ DX2/GPIO_74	O	1.8V	LCD B5 data bit when operating in 16 bpp 5:6:5 color mode. Please reference the *OMAP35x TRM* for 24-bit LCD bus mapping.
J1.220	uP_SPI_CS1	AG4	MMC2_DAT2/ McSPI3_CS1/ GPIO_134	O	1.8V	McSPI3 interface chip select 1 output.
J1.221	ONE_WIRE (BATT_LINE)	J25	HDQ_SIO/ SYS_ALTCLK/ I2C2_SCCBE/ I2C3_SCCBE/ GPIO_170	I/O	1.8V	Bi-directional battery management ONEWIRE interface. This signal has a 4.7K pull-up to VIO_1V8.
J1.222	uP_SPI_CS0	AF4	MMC2_DAT3/ McSPI3_CS0/ GPIO_135	O	1.8V	McSPI3 interface chip select 0 output.
J1.223	uP_SW_nRESET (SYS_nRESWARM)	(See Schematic)	(See Schematic)	I	1.8V	Active low. Input to CPU and power management controller. This signal has a 4.7K pull-up to VIO_1V8.
J1.224	uP_SPI_SOMI	AH5	MMC2_DAT0/ McSPI3_SOMI/ GPIO_132	I	1.8V	McSPI3 interface receive input.
J1.225	RESET_nOUT (SYS_nRESWARM)	(See Schematic)	(See Schematic)	O	1.8V	Active low. Reset output from the CPU that drives all onboard reset inputs. This signal should be used to drive reset inputs on external chips that require similar timing to the onboard devices. The SYS_nRESWARM signal has a 4.7K pull-up to VIO_1V8.
J1.226	uP_SPI_SIMO	AG5	MMC2_CMD/ McSPI3_SIMO/ GPIO_131	O	1.8V	McSPI3 interface transmit output.
J1.227	MSTR_nRST	AH25	SYS_ nRESPWRON	I	1.8V	Active low. External reset input to the OMAP35x SOM-LV. This signal should be used to reset all devices on the OMAP35x SOM-LV including the CPU.
J1.228	uP_SPI_SCLK	AE2	MMC2_CLK/ McSPI3_CLK/ GPIO_130	O	1.8V	McSPI3 serial clock signal.
J1.229	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J1.230	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J1.231	VMMC2	A4 (PMIC)	VMMC2.OUT (PMIC)	O	VMMC2	VMMC2 LDO output from TPS65950 available to user. Refer to the *TPS65950 TRM* for available voltages.

J1 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J1.232	TOUCH_nIRQ	AD1	McBSP4_DR/ SSI1_FLAG_RX/ HSUSB3_TLL_ DATA0/MM3_RXRCV/GPIO_153	O	1.8V	If touch chip is populated, this signal is the active low touch interrupt; do not connect. If touch chip is not populated, this signal is a processor GPIO available to user; connected to GPIO_153.
J1.233	WIRELESS_RS232_RX	—	—	I	1.8V	Used for test only. Do not connect.
J1.234	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.235	WIRELESS_RS232_TX	—	—	O	1.8V	Used for test only. Do not connect.
J1.236	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.237	DGND	(See Schematic)	(See Schematic)	I	DGND	Used for test only. Do not connect.
J1.238	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J1.239	WIRELESS_UART_DBG	—	—	O	1.8V	Used for test only. Do not connect.
J1.240	BT_TX_DBG	—	—	O	1.8V	Used for test only. Do not connect.

TABLE NOTES:

1. USB voltage levels follow the USB specification and depend on the USB operating speed. Please see the *USB 2.0 Specification* document for more information.

2. USB1_VBUS can be used to power the OMAP35x SOM-LV. Please see the *TPS65950 TRM* for more information.

3. Caution must be used when considering these signals for alternative functions as they may connect to the top PoP BGA footprint.

4. When using PoP memories with 16-bit NAND memory, these signals present an additional load on the GPMC bus that must be accounted for when calculating overall bus load.

7.2 J2 Connector 240-Pin Descriptions

J2 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J2.1	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J2.2	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J2.3	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J2.4	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J2.5	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.

J2 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J2.6	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J2.7	WLAN_nIRQ	AE1	McBSP4_CLKX/ SSI1_DAT_RX/ HSUSB3_TLL_ DATA1/ MM3_TXSE0/ GPIO_152	O	1.8V	If Ethernet chip is populated, this signal is the active low Ethernet interrupt; do not connect. If Ethernet chip is not populated, this signal is a processor GPIO available to user; connected to GPIO_152.
J2.8	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J2.9	ICT_TEST_MODE	A1 (PMIC)	TEST (PMIC)	I	1.8V	Used for test only. Do not connect.
J2.10	uP_CLKOUT2_ 26MHz	AE22	SYS_CLKOUT2/ GPIO_186	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_186.
J2.11	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J2.12	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J2.13	PCC_POWER_nEN (SIM0_VEN)	R27	MMC1_DAT6/ SIM_PWRCTRL/ GPIO_128	O	1.8V	Active low. Turns on power to CompactFlash/PC Card interface. This signal is also connected to J2.15 and J2.124.
J2.14	PCC_nOE (uP_nOE)	G2	GPMC_nOE	O	1.8V	Active low. CompactFlash/PC Card per transaction bus buffer Output Enable signal. This signal is also connected to J1.125.
J2.15	PCC_PCMCIA_nEN (SIM0_VEN)	R27	MMC1_DAT6/ SIM_PWRCTRL/ GPIO_128	O	1.8V	Active low. Enables CompactFlash control signals. This signal is also connected to J2.13 and J2.124.
J2.16	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J2.17	HSUSB1_D7	AE13	ETK_D3/ McSPI3_CLK/ MMC3_DAT3/ HSUSB1_DATA7/ HSUSB1_TLL_ DATA7/GPIO_17	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_17.
J2.18	uP_PCC_nWAIT	K8	GPMC_WAIT2/ GPIO_64	I	1.8V	Active low. CompactFlash/PC Card Wait signal.
J2.19	HSUSB1_D6	AF13	ETK_D6/ McBSP5_DX/ MMC3_DAT2/ HSUSB1_DATA6/ HSUSB1_TLL_ DATA6/GPIO_20	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_20.
J2.20	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J2.21	HSUSB1_D5	AH9	ETK_D5/ McBSP5_FSX/ MMC3_DAT1/ HSUSB1_DATA5/ HSUSB1_TLL_ DATA5/GPIO_19	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_19.

J2 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J2.22	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J2.23	HSUSB1_D4	AE11	ETK_D4/ McBSP5_DR/ MMC3_DAT0/ HSUSB1_DATA4/ HSUSB1_TLL_ DATA4/GPIO_18	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_18.
J2.24	uP_PCC_CD2 (uP_PCC_CD1)	AD2	McBSP4_DX/ SSI1_RDY_RX// HSUSB3_TLL_ DATA2/ MM3_TXDAT/ GPIO_154	I	1.8V	CompactFlash/ PC Card Detect 2 input. This signal is also connected to J2.26.
J2.25	HSUSB1_D3	AH14	ETK_D7/ McSPI3_CS1/ MMC3_DAT7/ HSUSB1_DATA3/ MM1_TXEN_n/ HSUSB1_TLL_ DATA3/GPIO_21	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_21.
J2.26	uP_PCC_CD1	AD2	McBSP4_DX/ SSI1_RDY_RX/ HSUSB3_TLL_ DATA2/ MM3_TXDAT/ GPIO_154	I	1.8V	CompactFlash/ PC Card Detect 1 input. This signal is also connected to J2.24.
J2.27	HSUSB1_D2	AH12	ETK_D2/ McSPI3_CS0/ HSUSB1_DATA2/ MM1_TXDAT/ HSUSB1_TLL_ DATA2/GPIO_16	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_16.
J2.28	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J2.29	HSUSB1_D1	AG12	ETK_D1/ McSPI3_SOMI/ HSUSB1_DATA1/ MM1_TXSE0/ HSUSB1_TLL_ DATA1/GPIO_15	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_15.
J2.30	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J2.31	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J2.32	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J2.33	HSUSB1_CLK	AE10	ETK_CTL/ MMC3_CMD/ HSUSB1_CLK/ HSUSB1_TLL_ CLK/GPIO_13	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_13.

J2 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J2.34	uP_PCC_RESET	AF19	SYS_BOOT4/ MMC2_DIR_DAT2/ GPIO_6	O	1.8V	CompactFlash/PC Card Reset output.
J2.35	HSUSB1_NXT	AG9	ETK_D9/ SYS_SECURE_ INDICATOR/ MMC3_DAT5/ HSUSB1_NXT/ MM1_RXDM/ HSUSB1_TLL_ NXT/GPIO_23	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_23.
J2.36	PCC_nDRV (uP_nCS3)	U8	GPMC_nCS3/ SYS_nDMAREQ0/GPIO_54	O	1.8V	CompactFlash/PC Card buffer Drive output. This signal is also connected to J2.48 and J2.50.
J2.37	HSUSB1_STP	AF10	ETK_CLK/ McBSP5_CLKX/ MMC3_CLK/ HSUSB1_STP/ MM1_RXDP/ HSUSB1_TLL_ STP/GPIO_12	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_12.
J2.38	PCC_nIOWR (VIO_1V8)	(See Schematic)	(See Schematic)	O	1.8V	Active low. CompactFlash/PC Card I/O Write output.
J2.39	HSUSB1_DIR	AF9	ETK_D8/ SYS_DRM_ MSECURE/ MMC3_DAT6/ HSUSB1_DIR/ HSUSB1_TLL_DIR/ GPIO_22	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_22.
J2.40	PCC_nWE (uP_nWE)	F4	GPMC_nWE	O	1.8V	Active low. CompactFlash/PC Card Write Enable output. This signal also connects to J1.127.
J2.41	HSUSB1_D0	AF11	ETK_D0/ McSPI3_SIMO/ MMC3_DAT4/ HSUSB1_DATA0/ MM1_RXRCV/ HSUSB1_TLL_ DATA0/GPIO_14	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_14.
J2.42	PCC_nIORD (VIO_1V8)	(See Schematic)	(See Schematic)	O	1.8V	Active low. CompactFlash/PC Card I/O Read output.
J2.43	HSUSB2_STP	AF7	ETK_D11/ HSUSB2_STP/ MM2_RXDP/ HSUSB2_TLL_ STP/GPIO_25	I/O	1.8V	If R71 populated, processor GPIO available to user; connected to GPIO_25. If R71 not populated, reserved for future use; do not connect.
J2.44	PCC_REG (uP_LA12)	—	—	O	1.8V	CompactFlash/PC Card Reg access output. This signal is also connected to J1.79.
J2.45	HSUSB2_D1	AH8	ETK_D15/ HSUSB2_DATA1/ MM2_TXSE0/ HSUSB2_TLL_ DATA1/GPIO_29	I/O	1.8V	If R71 populated, processor GPIO available to user; connected to GPIO_29. If R71 not populated, reserved for future use; do not connect.

J2 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J2.46	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J2.47	HSUSB2_D0	AG8	ETK_D14/ HSUSB2_DATA0/ MM2_RXRCV/ HSUSB2_TLL_ DATA0/GPIO_28	I/O	1.8V	If R71 populated, processor GPIO available to user; connected to GPIO_28. If R71 not populated, reserved for future use; do not connect.
J2.48	PCC_nCE1A (uP_nCS3)	U8	GPMC_nCS3/ SYS_nDMAREQ0/G PIO_54	O	1.8V	Active low. CompactFlash/PC Card Chip Enable 1A.This signal is also connected to J2.36 and J2.50.
J2.49	MCSPI_CS1 (HSUSB2_D3)	V3	McSPI2_CS1/ GPT8_PWM_EVT/ HSUSB2_TLL_ DATA3/ USUSB2_DATA3/ MM2_TXEN_N/ GPIO_182	I/O	1.8V	If R71 populated, processor GPIO available to user; connected to GPIO_182. If R71 not populated, reserved for future use; do not connect.
J2.50	PCC_nCE2A (uP_nCS3)	U8	GPMC_nCS3/ SYS_nDMAREQ0/G PIO_54	O	1.8V	Active low. CompactFlash/PC Card Chip Enable 2A. This signal is also connected to J2.36 and J2.48.
J2.51	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J2.52	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J2.53	MCSPI2_CS0 (HSUSB2_D6)	Y4	McSPI2_CS0/ GPT11_PWM_ EVT/ HSUSB2_TLL_ DATA6/ HSUSB2_DATA6/ GPIO_181	I/O	1.8V	If R70 populated, processor GPIO available to user; connected to GPIO_181. If R70 not populated, reserved for future use; do not connect.
J2.54	VREF_PCMCIA (VIO_1V8)	(See Schematic)	(See Schematic)	O	1.8V	CompactFlash/PC Card Voltage reference output.
J2.55	MCSPI2_SOMI (HSUSB2_D5)	Y3	McSPI2_SOMI/ GPT10_PWM_ EVT/HSUSB2_TLL_ DATA5/ HSUSB2_DATA5/ GPIO_180	I/O	1.8V	If R70 populated, processor GPIO available to user; connected to GPIO_180. If R70 not populated, reserved for future use; do not connect.
J2.56	A26 (uP_A10)	K3	GPMC_A10/ SYS_nDMAREQ3/G PIO_43	O	1.8V	Processor GPMC bus address bit 26. (See note 3)
J2.57	MCSPI2_SIMO (HSUSB2_D4)	Y2	McSPI2_SIMO/ GPT9_PWM_EVT/ HSUSB2_TLL_ DATA4/ HSUSB2_DATA4/ GPIO_179	I/O	1.8V	If R70 populated, processor GPIO available to user; connected to GPIO_179. If R70 not populated, reserved for future use; do not connect.
J2.58	USB4_nOC	—	—	I	3.3V (5V tolerant)	Active low. USB Host over current flag. Indicates to PHY an over current condition exists on the USB Host port.

J2 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J2.59	MCSPI2_CLK (HSUSB2_D7)	AA3	McSPI2_CLK/ HSUSB2_TLL_ DATA7/ HSUSB2_DATA7/ GPIO_178	I/O	1.8V	If R70 populated, processor GPIO available to user; connected to GPIO_178. If R70 not populated, reserved for future use; do not connect.
J2.60	USB4_PWR_nEN	—	—	O	3.3V	Active low. USB Host power enable. Enables power to the external USB power switch. This signal has a 10k pull-up to 3.3V. See example LV-Baseboard design for reference components.
J2.61	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J2.62	USB4_D+	—	—	I/O	Variable (See note 1)	USB Host port 4 I/O data plus signal. Route as differential pair with USB4_D-. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differential impedance.
J2.63	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J2.64	USB4_D-	—	—	I/O	Variable (See note 1)	USB Host port 4 I/O data minus signal. Route as differential pair with USB4_D+. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differential impedance.
J2.65	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J2.66	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J2.67	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J2.68	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J2.69	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J2.70	USB5_nOC	—	—	I	3.3V (5V tolerant)	Active low. USB Host over current flag. Indicates to PHY an over current condition exists on the USB Host port.
J2.71	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J2.72	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J2.73	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J2.74	USB5_D+	—	—	I/O	Variable (See note 1)	USB Host port 5 I/O data plus signal. Route as differential pair with USB5_D-. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differential impedance.
J2.75	VIBRA_M	G15(PMIC)	VIBRA.M (PMIC)	O	Max 4.3V (MAIN_BATTERY)	Vibrator M signal for H-Bridge operation.

J2 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J2.76	USB5_D-	—	—	I/O	Variable (See note 1)	USB Host port 5 I/O data minus signal. Route as differential pair with USB5_D+. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differential impedance.
J2.77	VIBRA_P	F15(PMIC)	VIBRA.P (PMIC)	O	Max 4.3V (MAIN_BATTERY)	Vibrator P signal for H-Bridge operation.
J2.78	USB5_PWR_nEN	—	—	O	3.3V	Active low. USB Host power enable. Enables power to the external USB power switch. This signal has a 10k pull-up to 3.3V. See example LV-Baseboard design for reference components.
J2.79	START.ADC	J9	START.ADC (PMIC)	I	1.8V	This signal is the TPS65950 ADC conversion request. When not used, connect to DGND.
J2.80	VREF_MMC/SD1 (VMMC1)	(See Schematic)	(See Schematic)	O	3.0V (VMMC1)	MMC/SD1 interface voltage reference output.
J2.81	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J2.82	SD1_DATA3	P28	MMC1_DAT3/ MS_DAT3/ GPIO_125	I/O	3.0V (VMMC1)	MMC/SD2 Data 3 signal. This signal has a 10K pull-up to VMMC1.
J2.83	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J2.84	SD1_DATA2	N25	MMC1_DAT2/ MS_DAT2/ GPIO_124	I/O	3.0V (VMMC1)	MMC/SD2 Data 2 signal. This signal has a 10K pull-up to VMMC1.
J2.85	uP_nWP	H1	GPMC_nWP/ GPIO_62	O	1.8V	Processor GPMC write protect signal. (See notes 3 & 4)
J2.86	SD1_DATA1	N26	MMC1_DAT1/ MS_DAT1/ GPIO_123	I/O	3.0V (VMMC1)	MMC/SD2 Data 1 signal. This signal has a 10K pull-up to VMMC1.
J2.87	uP_nADV_ALE	F3	GPMC_nADV_ALE	O	1.8V	Processor GPMC address valid or address latch enable signal. (See notes 2, 3, & 4)
J2.88	SD1_DATA0	N27	MMC1_DAT0/ MS_DAT0/ GPIO_122	I/O	3.0V (VMMC1)	MMC/SD2 Data 0 signal. This signal has a 10K pull-up to VMMC1.
J2.89	RFID_EN	A2 (PMIC)	RFID.EN (PMIC)	O	VMMC2 (programmable)	RFID device enable.
J2.90	SD1_CMD	M27	MMC1_CMD/ MS_BS/ GPIO_121	I/O	3.0V (VMMC1)	MMC/SD2 Command signal. This signal has a 10K pull-up to VMMC1.
J2.91	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J2.92	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J2.93	KEY_COL7	G4 (PMIC)	KPD.C7 (PMIC)	O	1.8V	Open drain. Keypad Column 7 signal.
J2.94	SD1_CLK	N28	MMC1_CLK/ MS_CLK/ GPIO_120	O	3.0V (VMMC1)	MMC/SD2 Clock signal. This signal has a 10K pull-up to VMMC1.

J2 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J2.95	KEY_COL6	H6 (PMIC)	KPD.C6 (PMIC)	O	1.8V	Open drain. Keypad Column 6 signal.
J2.96	VREF_I2C3 (VIO_1V8)	(See Schematic)	(See Schematic)	O	1.8V	I2C channel 3 voltage reference output.
J2.97	KEY_COL5	F4 (PMIC)	KPD.C5 (PMIC)	O	1.8V	Open drain. Keypad Column 5 signal.
J2.98	uP_I2C3_SCL	AF14	I2C3_SCL/ GPIO_184	I/O	1.8V	I2C channel 3 Clock signal. This signal has a 4.7K pull-up to VIO_1V8.
J2.99	KEY_COL4	G7 (PMIC)	KPD.C4 (PMIC)	O	1.8V	Open drain. Keypad Column 4 signal.
J2.100	uP_I2C3_SDA	AG14	I2C3_SDA/ GPIO_185	I/O	1.8V	I2C channel 3 Data signal. This signal has a 4.7K pull-up to VIO_1V8.
J2.101	KEY_COL3	F7 (PMIC)	KPD.C3 (PMIC)	O	1.8V	Open drain. Keypad Column 3 signal.
J2.102	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J2.103	KEY_COL2	G6 (PMIC)	KPD.C2 (PMIC)	O	1.8V	Open drain. Keypad Column 2 signal.
J2.104	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J2.105	KEY_COL1	H7 (PMIC)	KPD.C1 (PMIC)	O	1.8V	Open drain. Keypad Column 1 signal.
J2.106	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J2.107	KEY_COL0	G8 (PMIC)	KPD.C0 (PMIC)	O	1.8V	Open drain. Keypad Column 0 signal.
J2.108	uP_TMS	AA18	JTAG_TMS_TMSC	I	1.8V	CPU JTAG Test Mode Signal.
J2.109	KEY_ROW7	L7 (PMIC)	KPD.R7 (PMIC)	I	1.8V	Keypad Row 7 signal.
J2.110	uP_TCK	AA13	JTAG_TCK	I	1.8V	CPU JTAG Test Clock input signal.
J2.111	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J2.112	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J2.113	KEY_ROW6	K10(PMIC)	KPD.R6 (PMIC)	I	1.8V	Keypad Row 6 signal.
J2.114	uP_TDO	AA19	JTAG_TDO	O	1.8V	CPU JTAG Test Data Output from the CPU to the JTAG device.
J2.115	KEY_ROW5	J10 (PMIC)	KPD.R5 (PMIC)	I	1.8V	Keypad Row 5 signal.
J2.116	uP_nTRST	AA17	JTAG_nTRST	I	1.8V	CPU JTAG Test Reset input.
J2.117	KEY_ROW4	L9 (PMIC)	KPD.R4 (PMIC)	I	1.8V	Keypad Row 4 signal.
J2.118	uP_TDI	AA20	JTAG_TDI	I	1.8V	CPU JTAG Test Data Input to the CPU from the JTAG device.
J2.119	KEY_ROW3	K7 (PMIC)	KPD.R3 (PMIC)	I	1.8V	Keypad Row 3 signal.
J2.120	uP_RTCK	AA12	JTAG_RTCK	O	1.8V	CPU JTAG Return Test Clock signal.
J2.121	KEY_ROW2	L8 (PMIC)	KPD.R2 (PMIC)	I	1.8V	Keypad Row 2 signal.
J2.122	VREF_JTAG (VIO_1V8)	(See Schematic)	(See Schematic)	O	1.8V	CPU JTAG reference voltage output.

J2 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J2.123	KEY_ROW1	K8 (PMIC)	KPD.R1 (PMIC)	I	1.8V	Keypad Row 1 signal.
J2.124	SIM0_VEN	R27	MMC1_DAT6/ SIM_PWRCTRL/ GPIO_128	O	1.8V (VSIM)	Smart card voltage enable. **NOTE:** The OMAP35x processor does not natively support the SIM interface. This signal can be used as a GPIO. This signal is also connected to J2.13 and J2.15.
J2.125	KEY_ROW0	K9 (PMIC)	KPD.R0 (PMIC)	I	1.8V	Keypad Row 0 signal.
J2.126	SIM0_nDETECT	Y21	McBSP1_CLKR/ McSPI4_CLK/ SIM_CD/ GPIO_156	I	1.8V (VSIM)	Smart card detect. **NOTE:** The OMAP35x processor does not natively support the SIM interface. This signal can be used as a GPIO.
J2.127	CSI_HSYNC	A24	CAM_HS/ SSI2_DAT_TX/ GPIO_94	I/O	1.8V	Camera Sensor Interface Horizontal Sync signal.
J2.128	SIM0_CLK	P26	MMC1_DAT5/ SIM_CLK/ GPIO_127	O	1.8V (VSIM)	Smart card clock output. **NOTE:** The OMAP35x processor does not natively support the SIM interface. This signal can be used as a GPIO.
J2.129	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J2.130	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J2.131	CSI_VSYNC	A23	CAM_VS/ SSI2_FLAG_TX/ GPIO_95	I/O	1.8V	Camera Sensor Interface Vertical Sync signal.
J2.132	SIM0_IO/TX	P27	MMC1_DAT4/ SIM_IO/GPIO_126	I/O	1.8V (VSIM)	Smart card data in/out signal. **NOTE:** The OMAP35x processor does not natively support the SIM interface. This signal can be used as a GPIO.
J2.133	CSI_D0	AG17	CAM_D0/ CSI2_DX2/ GPIO_99	I	1.8V (VAUX4 – See note 5)	Camera Sensor Interface Data bit 0. This signal can be used as a GPI; output signaling is not supported.
J2.134	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J2.135	CSI_D1	AH17	CAM_D1/ CSI2_DY2/ GPIO_100	I	1.8V (VAUX4 – See note 5)	Camera Sensor Interface Data bit 1. This signal can be used as a GPI; output signaling is not supported.
J2.136	SIM0_nRESET	R25	MMC1_DAT7/ SIM_RST/ GPIO_129	O	1.8V (VSIM)	Smart card reset. **NOTE:** The OMAP35x processor does not natively support the SIM interface. This signal can be used as a GPIO.
J2.137	CSI_D2	B24	CAM_D2/ SSI2_RDY_TX/ GPIO_101	I	1.8V	Camera Sensor Interface Data bit 2.
J2.138	VREF_SIM (VSIM)	P25	VDDS_SIM	O	1.8V (VSIM)	Smart card reference voltage. Connected to VIO_1V8 through a 0 ohm resistor.
J2.139	CSI_D3	C24	CAM_D3/ SSI2_DAT_RX/ GPIO_102	I	1.8V	Camera Sensor Interface Data bit 3.

J2 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J2.140	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J2.141	CSI_D4	D24	CAM_D4/ SSI2_FLAG_RX/ GPIO_103	I	1.8V	Camera Sensor Interface Data bit 4.
J2.142	ICT_JTAG_TDO	—	—	O	1.8V	Used for test only. Do not connect.
J2.143	CSI_D5	A25	CAM_D5/ SSI2_RDY_RX/ GPIO_104	I	1.8V	Camera Sensor Interface Data bit 5.
J2.144	ICT_JTAG_TMS	N12 (PMIC)	GPIO.1/CD2/ JTAG.TMS (PMIC)	I	1.8V	Used for test only. Do not connect.
J2.145	CSI_D6	K28	CAM_D6/ GPIO_105	I	1.8V	Camera Sensor Interface Data bit 6.
J2.146	ICT_JTAG_TDI	A15(PMIC)	JTAG.TDI (PMIC)	I	1.8V	Used for test only. Do not connect.
J2.147	CSI_D7	L28	CAM_D7/ GPIO_106	I	1.8V	Camera Sensor Interface Data bit 7.
J2.148	ICT_JTAG_CLK	B16(PMIC)	JTAG.TCK (PMIC)	I	1.8V	Used for test only. Do not connect.
J2.149	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J2.150	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J2.151	CSI_D8	K27	CAM_D8/ GPIO_107	I	1.8V	Camera Sensor Interface Data bit 8.
J2.152	uP_GPIO_2	AA10	JTAG_EMU1/ GPIO_31	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_31. This signal is also connected to J1.166.
J2.153	CSI_D9	L27	CAM_D9/ GPIO_108	I	1.8V	Camera Sensor Interface Data bit 9.
J2.154	uP_GPIO_1	AA11	JTAG_EMU0/ GPIO_11	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_11. This signal is also connected to J1.216.
J2.155	CSI_D10	B25	CAM_D10/ SSI2_WAKE/ GPIO_109	I	1.8V	Camera Sensor Interface Data bit 10.
J2.156	BT_PCM_DX	C5 (PMIC)	GPIO.17/ BT.PCM.VDX/ DIG.MIC.CLK1 (PMIC)	I/O	1.8V	If Bluetooth populated, do not connect. If Bluetooth not populated, TPS65950 GPIO available to user. Connected to TPS65950 GPIO.17.
J2.157	CSI_D11	C26	CAM_D11/ GPIO_110	I	1.8V	Camera Sensor Interface Data bit 11.
J2.158	BT_PCM_DR	C3 (PMIC)	GPIO.16/ BT.PCMVDR/ DIG.MIC.CLK0 (PMIC)	I/O	1.8V	If Bluetooth populated, do not connect. If Bluetooth not populated, TPS65950 GPIO available to user. Connected to TPS65950 GPIO.16.
J2.159	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.

J2 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J2.160	BT_PCM_VFS	R16(PMIC) AE5	PCM.VFS (PMIC) McBSP3_FSX/ UART2_RX/ HSUSB3_TLL_ DATA7/GPIO_143	I/O	1.8V	If Bluetooth populated, do not connect. If Bluetooth not populated, Processor GPIO available to user. Connected to GPIO_143. **NOTE:** The TPS65950 PCM signal needs to be put in Tri-state mode.
J2.161	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J2.162	PCM_DX	T15(PMIC) AE6	PCM.VDX (PMIC) McBSP3_DR/ UART2_RTS/ HSUSB3_TLL_ DATA5/GPIO_141	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_141. **NOTE:** The TPS65950 PCM signal needs to be put in Tri-state mode.
J2.163	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J2.164	PCM_DR	T2 (PMIC) AF6	PCM.VDR (PMIC) McBSP3_DX/ UART21_CTS/ HSUSB3_TLL_ DATA4/GPIO_140	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_140. **NOTE:** The TPS65950 PCM signal needs to be put in Tri-state mode.
J2.165	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J2.166	BT_PCM_CLK	R1 (PMIC) AF5	PCM.VCK (PMIC) McBSP3_CLKX/ UART2_TX/ HSUSB3_TLL_ DATA6/GPIO_142	I/O	1.8V	If Bluetooth populated, do not connect. If Bluetooth not populated, Processor GPIO available to user. Connected to GPIO_142. **NOTE:** The TPS65950 PCM signal needs to be put in Tri-state mode.
J2.167	CSI_MCLK	C25	CAM_XCLKA/ GPIO_96	I/O	1.8V	Camera Sensor Interface Master Clock signal.
J2.168	EXT_BOOT_nSELECT	—	—	I	1.8V	uP_nCS2 select signal (0 = external device, 1 = onboard NOR flash, if populated). This is accomplished by onboard logic: if signal EXT_BOOT_nSELECT is high, then NOR_nCS = uP_nCS2; if signal EXT_BOOT_nSELECT is low, then BOOT_nCS = uP_nCS2. This defaults to the onboard flash if left unconnected (pulled to 1.8V through a 10K resistor). **NOTE**: R57 must be populated to boot from NOR or an external device; in this case, uP_nCS0 is tied to the uP_nCS2 net.
J2.169	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J2.170	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J2.171	CSI_PCLK	C27	CAM_PCLK/ GPIO_97	I	1.8V	Camera Sensor Interface Pixel Clock signal.

J2 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J2.172	BOOT_nCS	—	—	O	1.8V	Active Low. This signal is connected to uP_nCS2 when EXT_BOOT_nSELECT is low. When EXT_BOOT_nSELECT is high, this signal is inactive. This signal has a 4.7K pull-up to VIO_1V8.
J2.173	VREF_CSI (VPLL2)	(See Schematic)	(See Schematic)	O	1.8V (VPLL2)	Camera Sensor Interface reference voltage output.
J2.174	LCD_D23	AC28	DSS_D23/ SDI_CLKN/ GPIO_93	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the *OMAP35x TRM* for LCD bus mapping.
J2.175	VAUX3	(See Schematic)	(See Schematic)	O	VAUX3	Auxiliary power supply used to supply 2.8V for the wireless circuit. If wireless is not populated, may be user programmed. Requires capacitance on the baseboard for stabilization; recommend 1uF or larger. Refer to the *TPS65950 TRM* for available voltages.
J2.176	LCD_D22	AC27	DSS_D22/ SDI_CLKP/ GPIO_92	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the *OMAP35x TRM* for LCD bus mapping.
J2.177	TWL_CLK256FS	T21 D13(PMIC)	McBSP_CLKS/ CAM_SHUTTER/ UART1_CTS/ GPIO_160 CLK256FS (PMIC)	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_160.
J2.178	LCD_D21	J26	DSS_D21/ SDI_STP/ McSPI3_CS0/ DSS_DATA3/ GPIO_91	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the *OMAP35x TRM* for LCD bus mapping.
J2.179	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J2.180	LCD_D20	E28	DSS_D20/ SDI_DEN/ McSPI3_SOMI/ DSS_DATA2/ GPIO_90	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the *OMAP35x TRM* for LCD bus mapping.
J2.181	CSI1_DY1	AH18	CSI2_DY1/ GPIO_115	I	1.8V (VAUX4 – See note 5)	Camera Serial Interface 2 data/clock input. Route as differential pair with CSI1_DX1. **NOTE:** The OMAP35x processor does not natively support the CSI2 interface. This signal can only be used as a GPI. Output signaling is not supported.
J2.182	LCD_D19	H25	DSS_D19/ SDI_HSYNC/ McSPI3_SIMO/ DSS_DATA1/ GPIO_89	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the *OMAP35x TRM* for LCD bus mapping.

J2 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J2.183	CSI1_DX1	AG18	CSI2_DX1/ GPIO_114	I	1.8V (VAUX4 – See note 5)	Camera Serial Interface 2 data/clock input. Route as differential pair with CSI1_DY1. **NOTE:** The OMAP35x processor does not natively support the CSI2 interface. This signal can only be used as a GPI. Output signaling is not supported.
J2.184	LCD_D18	H26	DSS_D18/ SDI_VSYNC/ McSPI3_CLK/ DSS_DATA0/ GPIO_88	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the *OMAP35x TRM* for LCD bus mapping.
J2.185	CSI1_DY0	AH19	CSI2_DY0/ GPIO_113	I	1.8V (VAUX4 – See note 5)	Camera Serial Interface 2 data/clock input. Route as differential pair with CSI1_DX0. **NOTE:** The OMAP35x processor does not natively support the CSI2 interface. This signal can only be used as a GPI. Output signaling is not supported.
J2.186	LCD_D17	H27	DSS_D17/ GPIO_87	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the *OMAP35x TRM* for LCD bus mapping.
J2.187	CSI1_DX0	AG19	CSI2_DX0/ GPIO_112	I	1.8V (VAUX4 – See note 5)	Camera Serial Interface 2 data/clock input. Route as differential pair with CSI1_DY0. **NOTE:** The OMAP35x processor does not natively support the CSI2 interface. This signal can only be used as a GPI. Output signaling is not supported.
J2.188	LCD_D16	G25	DSS_D16/ GPIO_86	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the *OMAP35x TRM* for LCD bus mapping.
J2.189	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J2.190	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J2.191	MCSPI1_SOMI	AA4	McSPI1_SOMI/ MMC2_DAT6/ GPIO_173	I/O	1.8V	If Bluetooth populated, do not connect. If Bluetooth not populated, Processor GPIO available to user; connected to GPIO_173.
J2.192	TV_OUT2	W28	TV_OUT2	O	1.8V (VDAC)	Analog TV_OUT2.
J2.193	T2_REGEN	A10(PMIC)	REGEN (PMIC)	O	Max 4.3V (MAIN_BATTERY)	Active high. External LDO enable signal generated by the TPS65950.
J2.194	TV_OUT1	Y28	TV_OUT1	O	1.8V (VDAC)	Analog TV_OUT1.
J2.195	ADCIN6	N9 (PMIC)	ADCIN6 (PMIC)	I	max 2.7V	Analog to digital converter input. Connected to TPS65950 ADCIN6. When not used, leave floating.
J2.196	ADCIN2	G3 (PMIC)	ADCIN2 (PMIC)	I	1.5V	Analog to digital converter input. Connected to TPS65950 ADCIN2. When not used, connect to DGND.

J2 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J2.197	WLAN_MMC3_DATA3	AE3	MMC2_DAT7/ MMC2_CLKIN/ MMC3_DAT3/ HSUSB3_TLL_NXT/ MM3_RXDM/ GPIO_139	I/O	1.8V	If 802.11 populated, do not connect. If 802.11 not populated, Processor GPIO available to user; connected to GPIO_139.
J2.198	ADCIN1	J3 (PMIC)	ADCIN1 (PMIC)	I	1.5V	Analog to digital converter input. Connected to TPS65950 ADCIN1. When not used, connect to DGND.
J2.199	WLAN_MMC3_DATA2	AF3	MMC2_DAT6/ MMC2_DIR_CMD/ CAM_SHUTTER/ MMC3_DAT2/ HSUSB3_TLL_DIR/GPIO_138	I/O	1.8V	If 802.11 populated, do not connect. If 802.11 not populated, Processor GPIO available to user; connected to GPIO_138.
J2.200	ADCIN0	H4 (PMIC)	ADCIN0 (PMIC)	I	1.5V	Analog to digital converter input. Connected to TPS65950 ADCIN0. When not used, connect to DGND.
J2.201	WLAN_MMC3_DATA1	AH3	MMC2_DAT5/ MMC2_DIR_DAT1/ CAM_GLOBAL_RESET/ MMC3_DAT1/ HSUSB3_TLL_STP/ MM3_RXDP/ GPIO_137	I/O	1.8V	If 802.11 populated, do not connect. If 802.11 not populated, Processor GPIO available to user; connected to GPIO_137.
J2.202	IHF_RIGHT_M	B12(PMIC)	IHF.RIGHT.M (PMIC)	O	Max 4.3V (MAIN_BATTERY)	Hands-free speaker output right (M).
J2.203	WLAN_MMC3_DATA0	AE4	MMC2_DAT4/ MMC2_DIR_DAT0/ MMC3_DAT0/ GPIO_136	I/O	1.8V	If 802.11 populated, do not connect. If 802.11 not populated, Processor GPIO available to user; connected to GPIO_136.
J2.204	IHF_RIGHT_P	B11(PMIC)	IHF.RIGHT.P (PMIC)	O	Max 4.3V (MAIN_BATTERY)	Hands-free speaker output right (P).
J2.205	WLAN_MMC3_CMD	AC3	McSPI1_CS1/ ADPLLV2D_DITHERING_EN2/ MMC3_CMD/ GPIO_175	I/O	1.8V	If 802.11 populated, do not connect. If 802.11 not populated, Processor GPIO available to user; connected to GPIO_175.
J2.206	IHF_LEFT_M	B10(PMIC)	IHF.LEFT.M (PMIC)	O	Max 4.3V (MAIN_BATTERY)	Hands-free speaker output left (M).
J2.207	WLAN_MMC3_CLK	AB1	McSPI1_CS2/ MMC3_CLK/ GPIO_176	I/O	1.8V	If 802.11 populated, do not connect. If 802.11 not populated, Processor GPIO available to user; connected to GPIO_176.
J2.208	IHF_LEFT_P	B9 (PMIC)	IHF.LEFT.P (PMIC)	O	Max 4.3V (MAIN_BATTERY)	Hands-free speaker output right (P).
J2.209	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J2.210	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.

J2 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J2.211	MCSPI1_CLK	AB3	McSPI1_CLK/ MMC2_DAT4/ GPIO_171	I/O	1.8V	If Bluetooth populated, do not connect. If Bluetooth not populated, Processor GPIO available to user; connected to GPIO_171.
J2.212	MIC_IN	E3 (PMIC)	HSMIC.P (PMIC)	I	max 2.7V	Microphone input.
J2.213	MCSPI1_SIMO	AB4	McSPI1_SIMO/ MMC2_DAT5/ GPIO_172	I/O	1.8V	If Bluetooth populated, do not connect. If Bluetooth not populated, Processor GPIO available to user; connected to GPIO_172.
J2.214	MIC_SUB_M	H2 (PMIC)	MIC.SUB.M/ DIG.MIC.1 (PMIC)	I	2.2V (MICBIAS2)	Main microphone right input (M).
J2.215	MCSPI1_CS0	AC2	McSPI1_CS0/ MMC2_DAT7/ GPIO_174	I/O	1.8V	If Bluetooth populated, do not connect. If Bluetooth not populated, Processor GPIO available to user; connected to GPIO_174.
J2.216	MIC_SUB_P	G2 (PMIC)	MIC.SUB.P/ DIG.MIC.0 (PMIC)	I	2.2V (MICBIAS2)	Main microphone right input (P).
J2.217	MICBIAS2	D2 (PMIC)	MICBIAS2.OUT/ VMIC2.OUT (PMIC)	O	2.2V (MICBIAS2)	Analog microphone bias 2.
J2.218	MIC_MAIN_M	F2 (PMIC)	MIC.MAIN.M (PMIC)	I	2.2V (MICBIAS1)	Main microphone left input (M).
J2.219	MICBIAS1	D1 (PMIC)	MICBIAS1.OUT/ VMIC1.OUT (PMIC)	O	2.2V (MICBIAS1)	Analog microphone bias 1.
J2.220	MIC_MAIN_P	E2 (PMIC)	MIC.MAIN.P (PMIC)	I	2.2V (MICBIAS1)	Main microphone left input (P).
J2.221	MCBSP2_CLKX	L3 (PMIC) N21	I2S.CLK/ TDM.CLK (PMIC) McBSP2_CLKX/ GPIO_117	I/O	1.8V	If using audio, do not connect. If not using audio, Processor GPIO available to user; connected to GPIO_117.
J2.222	CODEC_INL	F1 (PMIC)	AUXL (PMIC)	I	max 2.7V	Auxiliary left channel line in.
J2.223	MCBSP2_FSX	K6 (PMIC) P21	I2S.SYNC/ TDM.SYNC (PMIC) McBSP2_FSX/ GPIO_116	I/O	1.8V	If using audio, do not connect. If not using audio, Processor GPIO available to user; connected to GPIO_116.
J2.224	CODEC_INR	G1 (PMIC)	AUXR (PMIC)	I	max 2.7V	Auxiliary right channel line in.
J2.225	MCBSP2_DR	K3 (PMIC) R21	I2S.DOUT/ TDM.DOUT (PMIC) McBSP2_DR/ GPIO_118	I/O	1.8V	If using audio, do not connect. If not using audio, Processor GPIO available to user; connected to GPIO_118.
J2.226	CODEC_OUTL	B4 (PMIC)	HSOL (PMIC)	O	max 2.7V	Left channel headset out.
J2.227	MCBSP2_DX	K4 (PMIC) M21	I2S.DIN/ TDM.DIN (PMIC) McBSP2_DX/ GPIO_119	I/O	1.8V	If using audio, do not connect. If not using audio, Processor GPIO available to user; connected to GPIO_119.
J2.228	CODEC_OUTR	B5 (PMIC)	HSOR (PMIC)	O	max 2.7V	Right channel headset out.
J2.229	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.
J2.230	DGND	(See Schematic)	(See Schematic)	I	GND	Ground. Connect to digital ground.

J2 Pin#	Signal Name	BGA Ball #	Processor Signal	I/O	Voltage	Description
J2.231	T2_CLKREQ	AF25 G10(PMIC)	SYS_CLKREQ/ GPIO_1 CLKREQ (PMIC)	I/O	NA	Reserved for future use. Do not connect.
J2.232	BT_IRQ	AA21	McBSP1_FSR/ CAM_GLOBAL_ RESET/ ADPLLV2D_ DITHERING_EN1/ GPIO_157	I/O	1.8V	If Bluetooth populated, do not connect. If Bluetooth not populated, Processor GPIO available to user; connected to GPIO_157.
J2.233	uP_CLKOUT1_ 26MHz	AG25	SYS_CLKOUT1/ GPIO_10	O	1.8V	Processor SYS_CLKOUT1. **NOTE:** This signal is shared with Bluetooth and should not be used off-board if Bluetooth is required.
J2.234	TWL_32K_CLK _OUT	N10(PMIC) AE25	32KCLKOUT (PMIC) SYS_32K	O	1.8V	TPS65950 32kHz clock output.
J2.235	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J2.236	RFU	—	—	I/O	NA	Reserved for future use. Do not connect.
J2.237	VDD2_CORE	—	—	O	1.2V	Used for test only. Do not connect.
J2.238	VDD1_CORE	—	—	O	1.2V	Used for test only. Do not connect.
J2.239	NOR_nCS	—	—	O	1.8V	Used for test only. Do not connect.
J2.240	TWL_CLKEN	—	—	I	1.8V	Used for test only. Do not connect.

TABLE NOTES:

1. USB voltage levels follow the USB specification and depend on the USB operating speed. Please see the *USB Specification 2.0* document for more information.

2. On the OMAP35x SOM-LV, uP_nADV_ALE is used to control a transparent D-type latch. When uP_nADV_ALE is high, the address lines flow through the latch; when uP_nADV_ALE is low, the address lines are latched. Because of this setup, uP_nADV_ALE should be set high for one clock at the beginning of GPMC cycles and transitioned low for the rest of the bus transaction to hold the address for the entire cycle. Please see diagrams in Section 4.2.3.1 for an example.

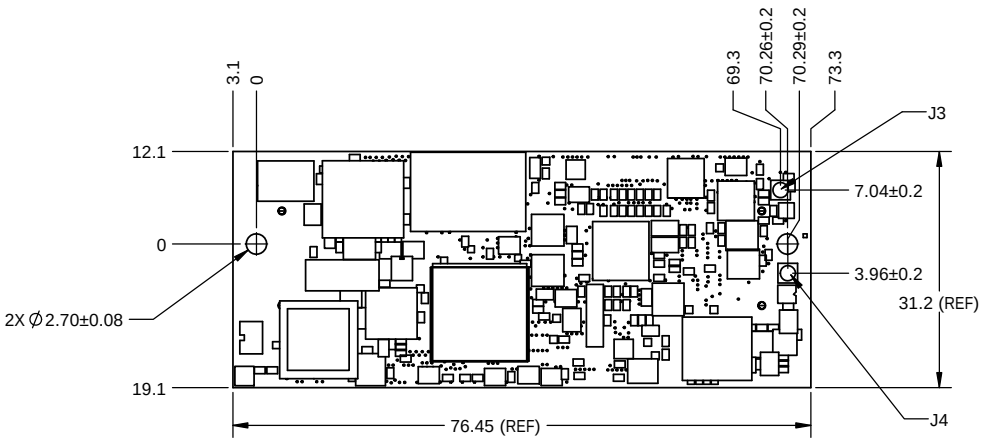
3. Caution must be used when considering these signals for alternative functions as they may connect to the top PoP BGA footprint.

4. When using PoP memories with 16-bit NAND memory, these signals present an additional load on the GPMC bus that must be accounted for when calculating overall bus load.

5. The VAUX4 supply is off by default and must be enabled by software.

Appendix A: Mechanical Drawings

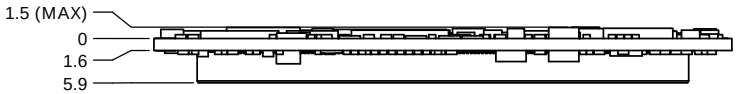
Revisions			
REV.	PCB	DESCRIPTION	DATE
D	1010946, 1015008,1017872	UPDATED FOR AM3703 & DM3730 MODELS, ADDED ETM DIMENSIONS	07.15.11
E	1010946, 1015008,1017872	ADDED ADDITIONAL PIN CALLOUTS ON FOOTPRINT	05.24.12

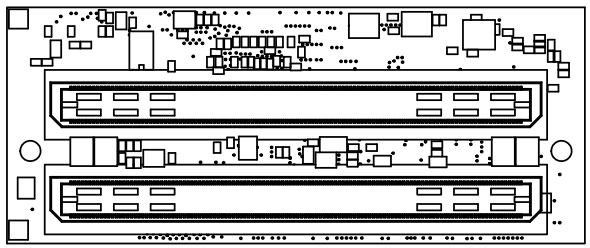


TOP

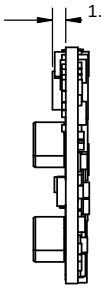
NOTES:

1. WITHIN LAYOUT AREA OF SOM-LV, MAXIMUM COMPONENT HEIGHT ON APPLICATION BASEBOARD IS 1.0 MM
2. BASEBOARD CONNECTOR SPECIFICATION: SAMTEC BSH-120-01-L-D-A
3. COMPONENT PLACEMENT IS FOR REFERENCE ONLY
4. DO NOT SCALE DRAWING





BOTTOM



THIS DRAWING PREPARED IN ACCORDANCE WITH ASME Y14.5-2000

ALL DIMENSIONS ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED

TOLERANCES UNLESS OTHERWISE SPECIFIED

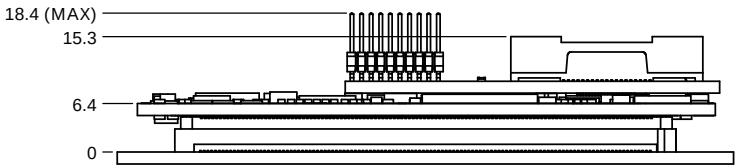
X	± 0.5
X.X	± 0.2
X.XX	± 0.1
X°	± 1°

THIRD ANGLE PROJECTION

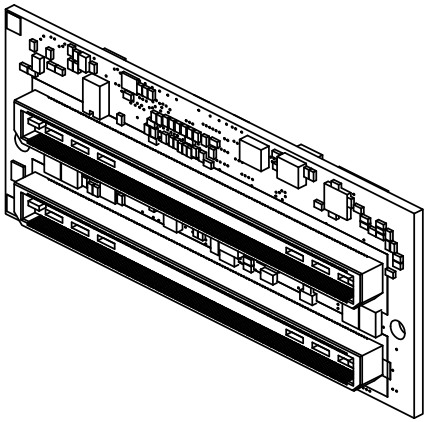
ENG NWR	DATE 07.15.11		
CHECK KAG	DATE 07.15.11		
MGR PMH	DATE 07.15.11		
MANF	DATE		

LOGIC PD
411 WASHINGTON AVE. SUITE 400 MINNEAPOLIS, MN 55401
T : 612.672.9495 F : 612.672.9489 I : WWW.LOGICPD.COM

SIZE	TITLE	REV
C	AM3703, DM3730 & OMAP35X SOM-LV	E
SCALE 2:1	DWG NO 1010498	SHEET 1 OF 2



PRODUCT HEIGHT WITH ETM DEBUG BOARD ATTACHED



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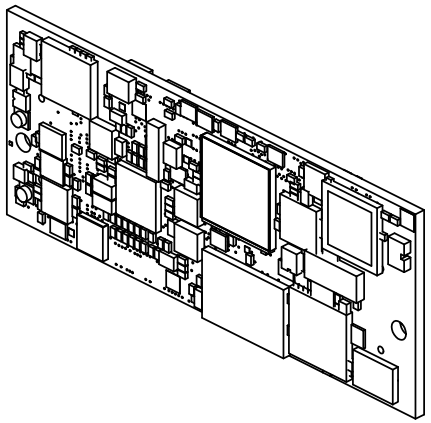
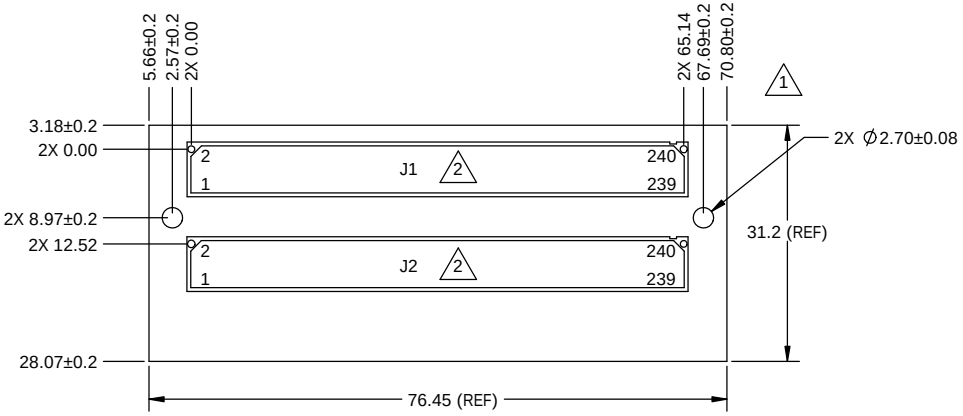


TOP

ISOMETRIC VIEWS FOR
REFERENCE ONLY



RECOMMENDED BASEBOARD FOOTPRINT

SIZE	TITLE	REV
C	AM3703, DM3730 & OMAP35X SOM-LV	E
SCALE 1:1	DWG NO 1010498	SHEET 2 OF 2